MICROPROCESSOR BASED PWM MODULATOR FOR THREE-PHASE INDUCTION MOTOR DRIVE

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of

MASTER OF TECHNOLOGY

by

VIJAY V. DESHPANDE

to the

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR
SEPTEMBER, 1984

CERTIFICATE

This is to certify that the thesis entitled, " MICROPROCESSOR BASED PWM MODULATOR FOR THREE PHASE INDUCTION MOTOR DRIVE " is a record of the work carried out under my supervision by Shri Vijay V. Deshpande and that it has not been submitted elsewhere for a degree.

(S.R. Doradla)
Assistant Professor
Department of Electrical Engineering
I.I.T. Kanpur

ACKNOWLEDGEMENTS

I would like to thank my thesis supervisor Dr.S.R.Doradla for his guidance and help throughout the project.

I take this opportunity to thank Prof. G.S. Buja of University of Padova (Italy) and Prof. F. Zach of Institut fur Allgemeine Elektrotechnik und Elektronik (Austria) for sending the optimal switching angles, without which this project could not have been completed.

I thank Dr. R.N. Biswas for making all the microcomputer facilities available to me, which were essential for the project. Also thanks to Dr. Sanjay Bose for his help, and to Dr. A.Joshi for his suggestions.

Here I thank Shri D.N. Joshi and Om Prakash Arora of power electronics lab for their immense help throughout the project. My thanks to Shri S.N. Kole, Ramsingh of PCB lab and and P.S. Tiwari of ACES workshop for making the tachometer successful. My thanks to Shri S.N.Sikdar for making available the power transistors, and to Shri Bhatnagar and R.P.Singh for their kind help and also to M.L.Gupta and S.P.Tyagi of EMEC lab.

Finally to my friends Mukund, Lt.Dutt,Chakravorty,ASN Murthy,Durgaprasad, Capt Pande, Bandopadhyay,Ashish,Biswajit, Sumit,Gautam,Islam I express my thanks for their pleasant company. Also to Shri R.G.Kale for his invaluable suggestions.

Lastly I thank Mrs. Kamla Devi for her neat and timely typi

IIT Kanpur
31.8.84

Vijay V. Deshpande

ABSTRACT

A microprocessor (8085 A) based multimode firing circuit suitable for a high performance PWM inverter - fed induction motor drive is proposed. Sinusoidal and optimal PWM are implemented using the firing scheme in the low frequency range, while square wave operation is realized in the high frequency range. Frequency resolution of better than 0.038 Hz and voltage jump of less than 0.5% are achieved. Any voltage to frequency law can be implemented by simply changing the look-up-table. All functions except digital comparison have been implemented in software making the scheme reliable, flexible and economical. The availability of CPU time for closed loop calculations has been discussed. The harmonic spectrum analysis of waveforms has revealed a good agreement between the experimental and the simulation results. Finally the firing scheme has been tested for the speed torque characteristic on a single phase induction motor using a transistorised power inverter.

CONTENTS

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The ac machines were commonly employed, till early sixties, for fixed speed applications, since the speed changing apparatus was quite elaborate. The dc machines were used for variable speed applications, since they provided versatile speed torque characteristics. But dc machines are costlier, need regular maintainance due to the presence of brush and commutators, and are unsuitable for dusty and explosive environments. It has been found that major portion of electricity generated is consumed by electrical machines. The dc machines consume less than 10% of this energy, and the rest of the energy is consumed by ac machines. If ac variable speed drives were judiciously used, a substantial amount of energy can be saved.

All these factors motivated research in variable speed ac drives. Many schemes have been developed for the speed control of ac machines, of all such schemes, the inverter with frequency control provided versatile characteristics. But the cost of the controller of an ac drive is considerably higher and the control is far more complex than for a dc drive. With the rapid developments in power semiconductor devices, cheaper

and better devices are being made available. Two such devices are power transistors and MOSFETS. These are fast switching devices and have simpler commutation processes. The costs of these devices are declining gradually. Along with power devices, the control circuitry also is being simplified because of the availability of LSI chips, and microcomputer systems. These will help implement very complicated control systems. All these developments have helped in reducing the costs of ac drives, and improve their performance.

Keeping in view these developments, the study of pulse width modulated (PWM) inverter fed induction motor drive was taken up. It is a variable frequency drive, with voltage, frequency and harmonics being controlled by switching technique within the inverter itself. This makes the firing circuit of the inverter quite complex. A mocrocomputer is used to generate the firing pulses. A single phase power transistor inverter was fabricated and tested on a single phase induction motor. Also a detailed spectrum analysis of waveform was done and compared with the experimental results.

1.2 ORGANIZATION OF THESIS

Chapter 2 contains a brief literature survey on PWM systems, different kinds of modulation techniques and their implementation on microcomputers. A complete PWM inverter drive scheme is also proposed.

Chapter 3 deals with the details of the firing circuit showing hardware and software requirements. The salient features of the circuit are discussed and the CPU time availability for closed loop calculations is studied.

The digital simulation of PWM waveforms along with the analysis is presented in chapter 4. The simulated results of the harmonic contents of PWM waveforms have been presented. Waveforms expected from both single-phase and three phase inverters have been considered in the study of harmonic analysis.

Chapter 5 gives the details of the snubber and driving circuit for a power transistor. The speed torque characteristics of a single-phase inverter driven induction motor are obtained. Also the experimental results relating to the turn off process of power transistor are presented. The comparison of experimental results with the simulated ones has been given. Also some oscillograms and harmonic spectra have been presented.

CHAPTER 2

LITERATURE SURVEY

2.1 INTRODUCTION

One way of changing the speed of an induction motor is by varying the frequency of the supply to the motor. The synchronous speed of the motor of P poles supplied with a voltage of frequency f is given by

$$N_S = \frac{120f}{P} \qquad (2.1)$$

But while changing the frequency the flux density should be maintained at an optimum level so as to obtain maximum torque A higher flux density will result in saturation of the core and increased losses while a lower flux density will reduce the torque output of the motor. The air-gap flux per pole ϕ, can be shown as,

$$\phi = K \frac{V}{f} \qquad (2.2)$$

Where V is the applied voltage at a frequency f, and K is the proportionality constant which depends upon the design parameters of the motor.

The expression (2.2) shows that in order to maintain ϕ constant, the ratio V/f should be kept constant. In practice the ratio, V/f is maintained constant up to the base frequency

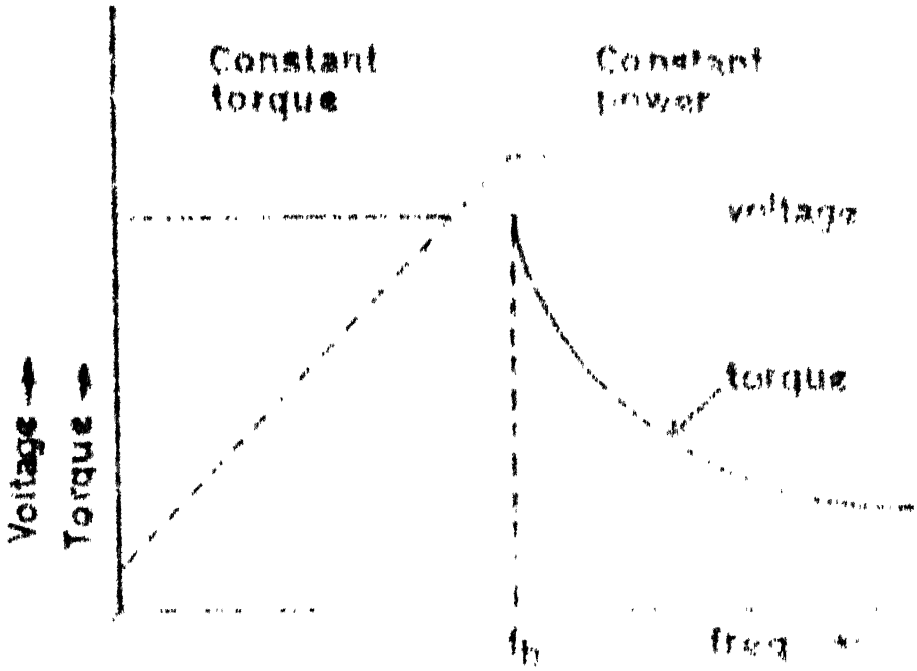


Fig 2.1 SPEED FORCE CHARACTERISTICS

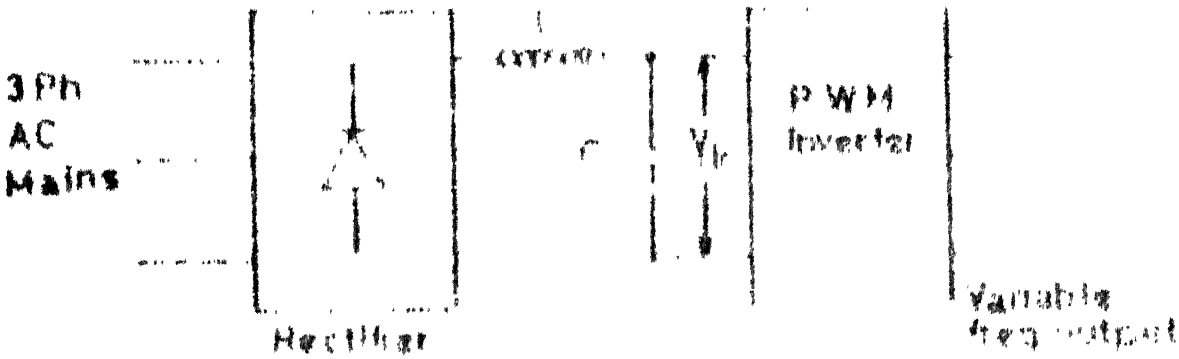


Fig 2.2 PWM DRIVE

at which the voltage reaches the rated value. Thus a constant torque is developed upto the base frequency. Further increase in the frequency is done at constant voltage, resulting in constant power drive. At very low frequencies, the stator resistance dominates the reactance, hence the voltage in this region is given a boost, to maintain the flux at the same level (fig. 2.1).

Two well known variable frequency induction motor drives are,

1. Voltage source inverter (VSI) drive
2. Current source inverter (CSI) drive.

The available ac mains is converted to dc and then inverted to variable frequency ac using either a VSI or a CSI. A large inductor is introduced in the dc link for a CSI. The current in a CSI or voltage to a VSI are controlled using a controlled rectifier. If a PWM (VSI) inverter is used, the voltage control is achieved by switching techniques within the inverter, and the dc link voltage is held constant as shown in fig. 2.2.

The square wave output contains a large number of harmonics. These harmonics have two unwanted effects on the operation of a motor. First, heating due to harmonics, and second torque pulsations at the motor shaft. Therefore it is

desirable that harmonic content of the waveform be minimum. By employing modulation techniques, it is possible to control the harmonics in the output of PWM inverter. Thus a PWM inverter not only controls frequency and voltage, but also the harmonic contents of the output waveform. In addition to this, a PWM inverter drive system offers some more advantages which are listed below.

1. The use of an uncontrolled rectifier in the front end reduces line voltage distortions and improves power factor. It requires a smaller filter and increases reliability of the system. With the constant dc link voltage more than one inverter can be independantly operated on the same dc bus, thus reducing costs. In a thyristor inverter through out the range of frequency, commutation is reliable.

2. Reduction in harmonics reduces torque pulsations, thus increasing the control range, practically from stand still with full torque capability.

3. A PWM inverter fed low inertia squirrel cage induction motor provides fast dynamic response.

4. If the DC link is capable of absorbing current (using other loads) then the regeneration can be easily incorporated in the drive thereby making it more versatile.

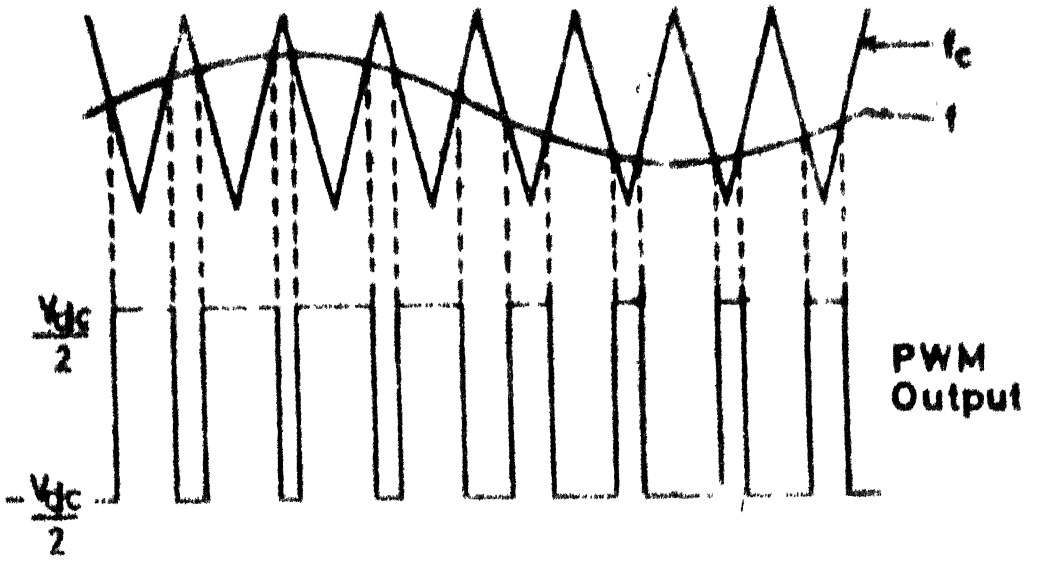


Fig 2.3 Natural PWM

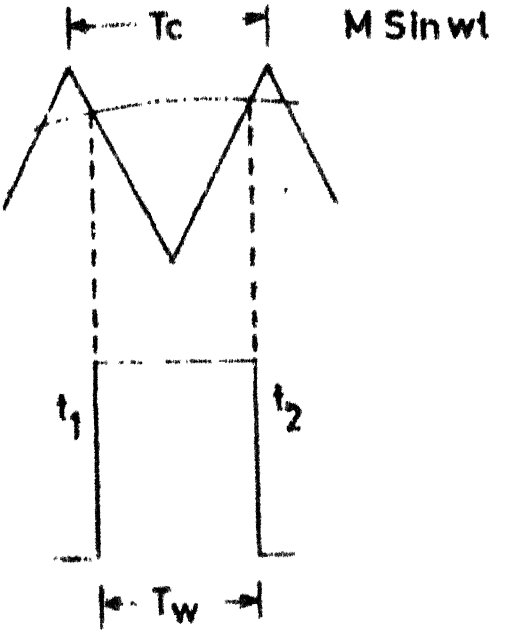


Fig 2.4

The disadvantage of a PWM inverter is that it's efficiency is lower, because of large number of switchings. A trade off between inverter losses and motor losses exists, which should be carefully decided in different ranges of frequencies.

2.2 PWM TECHNIQUES

There are different kinds of PWM techniques namely sinusoidal PWM, optimal PWM, harmonic elimination technique etc. Best possible performance can be obtained by choosing different techniques in different frequency ranges. A brief study of the above techniques is presented in the following section.

2.2.1 Sinusoidal Pulse Width Modulation

a) Natural sampled PWM :

If a triangular wave (called carrier f_c) is compared with a sine wave of reference frequency (f), then the resulting switched waveform is called sinusoidal PWM (SPWM) as shown in Fig. 2.3. This type of modulation is best suited for analog techniques, since the two frequencies are directly compared using comparators. But for microprocessor implementation, in which usually the pulse width is calculated by solving the modulation equation, this is unsuitable. The reason being, the natural PWM gives rise to a transcendental equation which is difficult to solve on µp's. From fig. 2.4, we get,

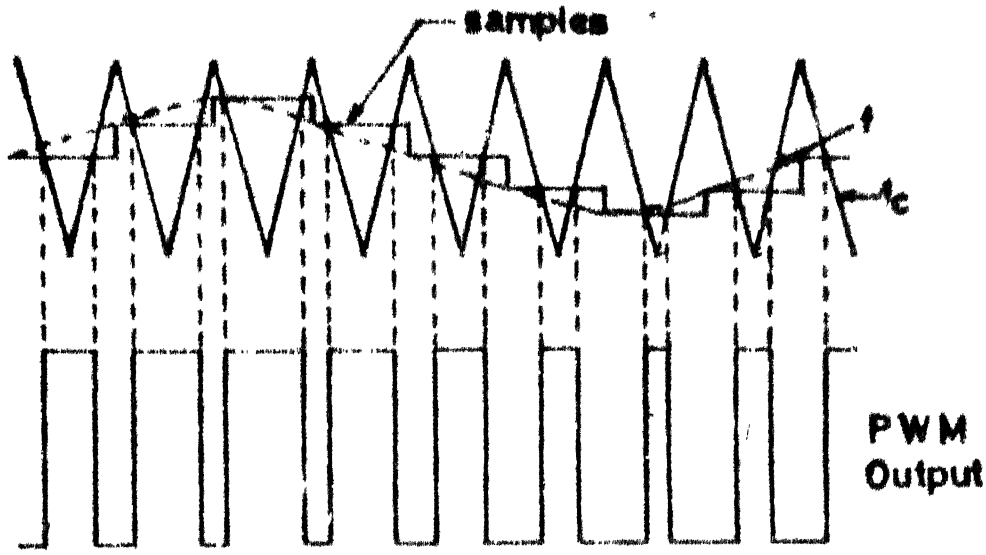


Fig 2.5 REGULAR PWM

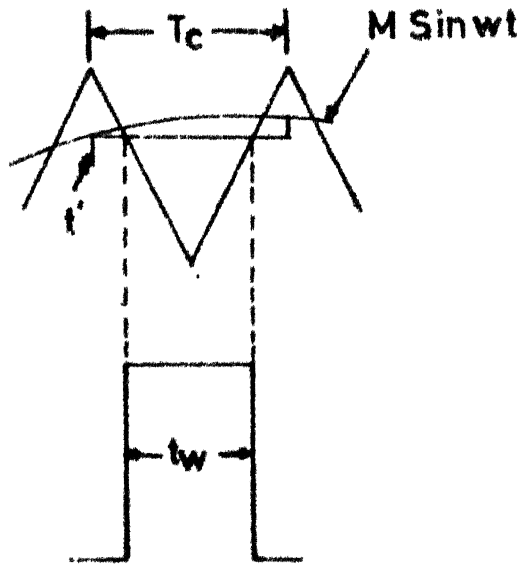


Fig 2.6

$$t_w = t_2 - t_1 = \frac{T_C}{2}\left[1 + \frac{M}{2}(\sin wt_1 + \sin wt_2)\right] \qquad (2.3)$$

To avoid this difficulty a regular PWM technique has been proposed [1], which is discussed below.

b) Regular sampled PWM :

In this technique the instantaneous sine value at the begining of carrier is sampled and held constant throughout the carrier. This generates a pulse width which is symmetrical within the carrier and its equation simplifies to (fig 2.6)

$$t_w = \frac{T_C}{2}\left[1 + M \sin(wt')\right] \qquad (2.4)$$

This technique is suitable for microcomputer implementation because equation (2.4) can be easily solved and requires one multiplication between M and sine sample. The value of T_C is chosen to be multiple of 2, so that it's multiplication reduces to a simple shift operation. Also instead of generating a sine wave, a sine table is stored in the memory and the samples are taken at regular intervals, depending upon the required frequency.

In SPWM, the choice of ratio f_c/f is important. A highest possible ratio is usually preferred, so that the spectrum of harmonics is shifted to higher values. Then the motor leakage inductance provides the filtering effect for

these harmonics. There are two distinct possibilities, the frequency ratio can be either fixed (Synchronous operation) or variable (asynchronous operation).

I) Synchronous SPWM :

In this method the carrier frequency is synchronously varied with reference frequency, and both are kept in phase. The ratio is usually chosen to be multiples of 3 so that in 3 phase waveforms, the multiples of third harmonic get cancelled. The actual value of f_c depends upon the switching speeds of devices used in the inverter.

II) Asynchronous operation :

Here the carrier is always held constant and the reference frequency is varied, so that the ratio increases as the reference frequency decreases. If this ratio is high then the frequencies need not be synchronised. The spectrum consists of harmonics which are multiples of f_c. Asynchronous SPWM is used for very low frequencies when motor speeds are low. In asynchronous operation the first highest harmonic frequency is f_c irrespective of the value of the reference frequency.

2.2.2 Optimal PWM

In optimal PWM additional switchings are introduced. This is illustrated in fig. 2.7 where m switching are introduced

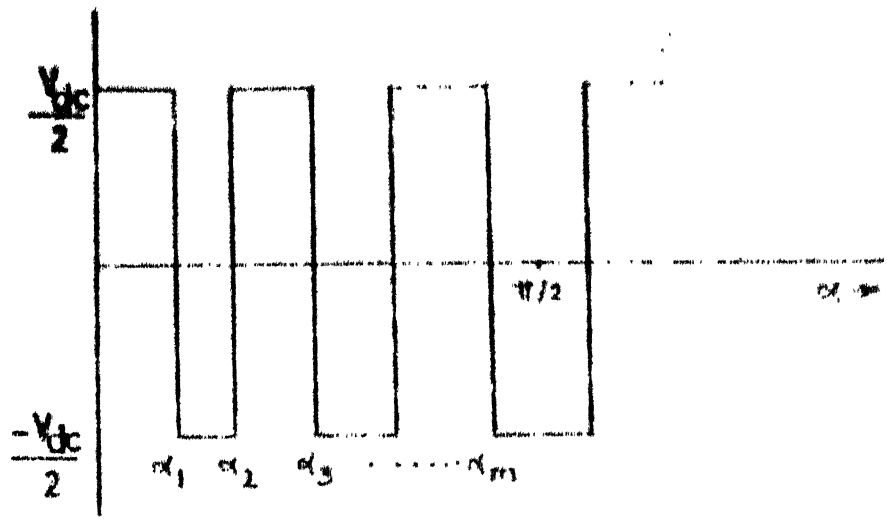


Fig 2.7 OPTIMAL PWM

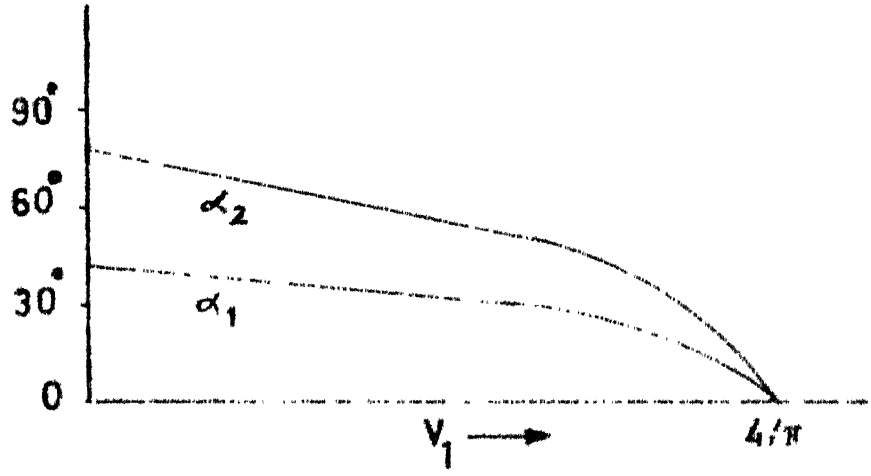


Fig 2.8 M = 2

between 0 and $\pi/2$. The angles α_1, α_2, ... α_m are determined, such that one constraint is used and some performance index is optimised. Usually one of the switchings is used to control the amplitude of the fundamental, while the rest of the switchings are used to minimize either harmonic currents, or torque pulsations, or any other performance quantity of interest. For a square wave the peak magnitude of the fundamental is,

$$V_1 = \frac{4}{\pi} \text{ per unit dc voltage}$$

V_1 can be varied from zero to $\frac{4}{\pi}$. The variation of V_1 for optimizing rms harmonic current with RL load and for m=2 is shown in fig 2.8 [5].

The value of m for which the optimization is done is usually limited to 4 or 5 since with each additional switching the optimization process becomes quite involved. For microprocessor implementation, these values are stored in a look up table.

2.2.3 Harmonic Elimination

The harmonic elimination technique is simillar to the optimal PWM. In this method, a band of harmonics of lower order are eliminated completely instead of optimizing [2]. Here too, one switching is used to control the amplitude of the fundamental.

2.3 COMPARISON

For a given harmonic content in the PWM waveform, optimal PWM gives the least number of switchings, per cycle. But the optimization becomes very complicated with switchings more than 4 to 5 per quarter cycle. Therefore whenever the harmonic content is to be better than that offered by the optimal PWM, the SPWM is adopted. The optimal PWM is usually preferred over harmonic elimination technique because of lesser harmonic contents for a given number of switchings.

2.4 PROPOSED SCHEME

It is proposed to develop a versatile microprocessor (8085A) based firing circuit with which the different PWM techniques discussed earlier can be implemented. The different PWM modes of operation and their frequency ranges which the firing scheme is capable of providing are shown in fig. 2.9. This multimode scheme was first proposed by B.K. Bose and H.A Sutherland [6].

In the low frequency range, the speed of the induction motor is low, and the cooling becomes quite ineffective. The use of SPWM, up to 20 Hz, which provides waveform with very low harmonic content, prevents the heating of the motor due to harmonic currents. So as to derive maximum advantage of SPWM, highest possible carrier frequency is chosen. The value of this

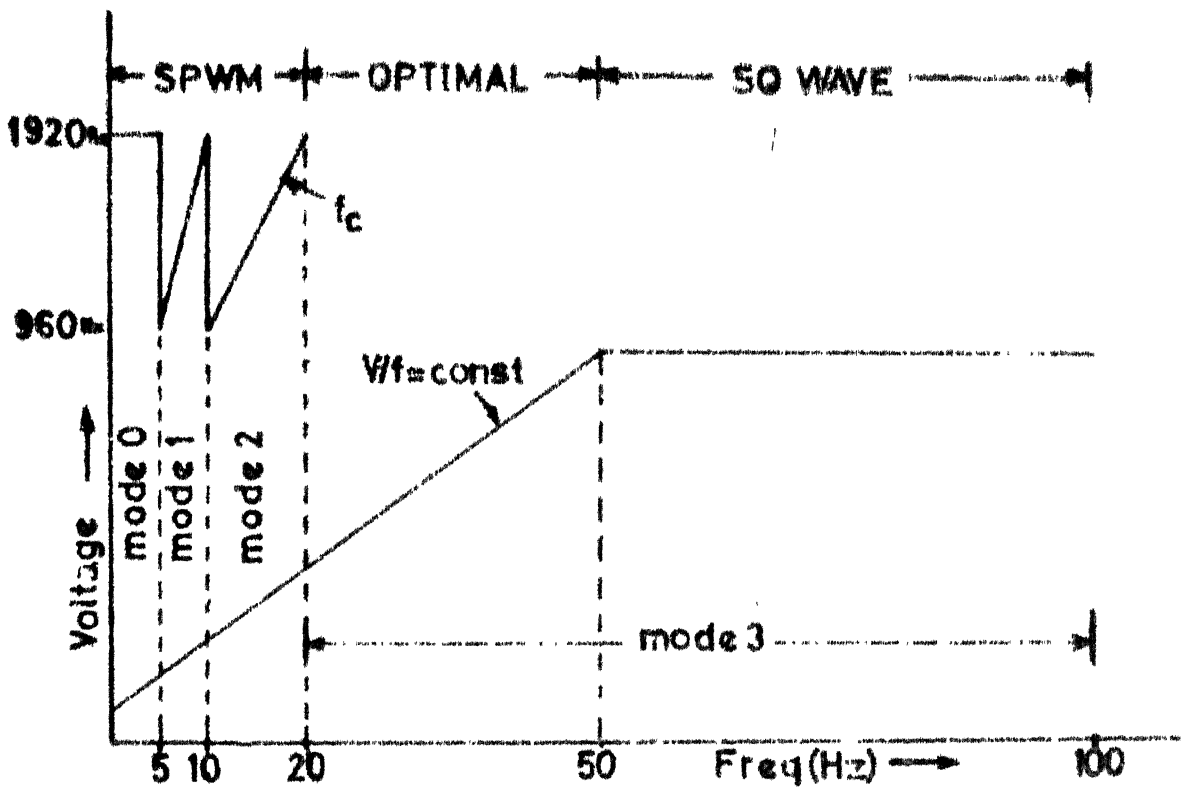


Fig 2.9 Multimode scheme

carrier frequency is then decided by the switching capabilities of the inverter. With the presently available thyristors, the operating frequencies are low. Power transistors are capable of operating at frequencies in excess of 6 KHz but the switching losses are directly related to frequency and these can become excessive at much lower frequencies than 6 KHz [17]. A carrier frequency around 2 KHz has been found suitable. Here the carrier was chosen to be 1920 Hz. In synchronous SPWM, the carrier varies along with the output frequency. This variation is from 960 Hz to 1920 Hz. In mode 1 frequency ratio is 192, hence 192 samples of sine wave are stored. In mode 2, the ratio is reduced to 96, and only the alternate samples are used. In asynchronous SPWM, frequency ratio, which is variable, exceeds 192. Due to limited number of samples, more than one carrier is generated per sample.

Beyond 20 Hz, optimal PWM is used. The number of switchings are greatly reduced reducing the switching losses. The harmonic content deteriorates to some extent. As the fundamental frequency is higher, and the cooling is also better, the effects of harmonic become less severe. The optimal PWM at 50 Hz becomes a square wave. At this point, the motor gets rated voltage, which is maintained constant beyond 50 Hz. A square wave operation gives the benefit of maximum utilization of DC link voltage.

2.5 CLOSED LOOP CONTROL

A block diagram of a controlled slip drive is given in fig. 2.10. A speed loop has been incorporated. The difference in reference speed and the actual speed fed to the speed regulator. The error, which represents the slip, is limited to the a value below pull out torque. The output of speed regulator is added to the actual speed of motor. The resulting sum determines the operating frequency of the inverter. The frequency command also generates the voltage command to the inverter.

An optical tachometer can be used as a speed transducer. The output of an optical tachometer being in the form of pulses, can be fed to a counter for a known duration. The speed then can be read from the counter. An optical tachometer has been fabricated for this purpose in the laboratory (see appendix D). It gives 1440 pulses per rpm.

The other functions of closed loop can be easily implemented in the software itself, employing sampled data control system.

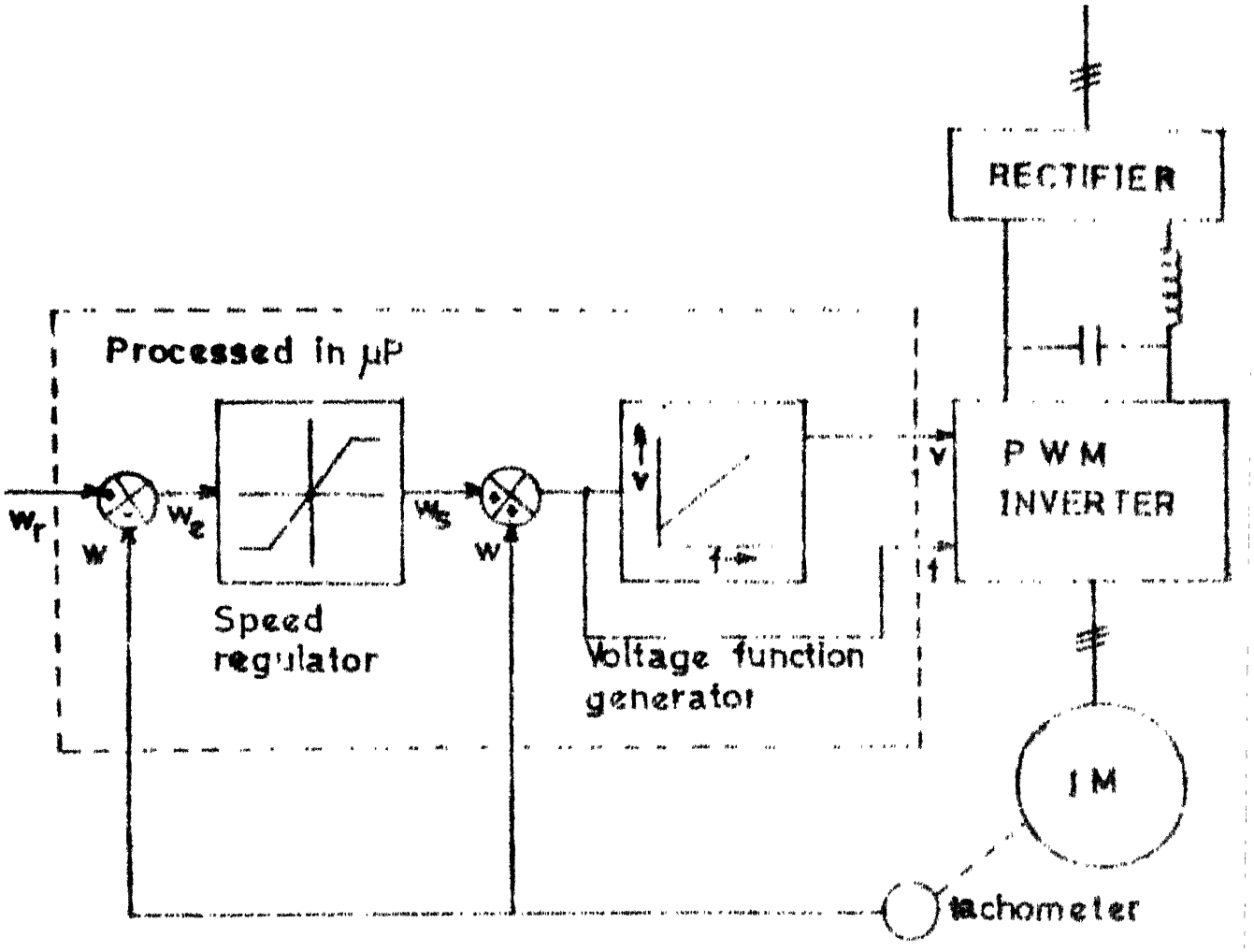


Fig 2.10 Controlled slip drive

CHAPTER 3

FIRING CIRCUIT IMPLEMENTATION

3.1 INTRODUCTION

Before the availability of microprocessors, some attempts were made to implement the PWM control circuits using analog components. Now because of the distinct advantages of a microprocessor, there is a total shift towards implementing these schemes on microprocessor based system. It offers improved reliability, flexibility, multiple control functions etc. Therefore only the study of μP based system is taken up here.

Generally in sinusoidal PWM (SPWM) the pulses are generated by on line computation based on regular SPWM. Whereas in optimal PWM look up table method is used. Irrespective of the type of modulation, the generation of pulse width can be done in two distinct ways. In one method [6,7] there is one counter per phase, and the delays for that particular phase are generated using respective counters. Each counter generates an interrupt. In the other method [8], only one counter is used, and the status of each phase is represented by one bit at the output port. The time delays for which the status of all three phases are constant, are generated by the single counter. The delays can either be calculated or stored in a table.

B.K. Bose and H.A. Sutherland [6] proposed a multimode system in which different modes are implemented for different ranges of frequency. For the range of frequency 0.5 Hz to 20 Hz SPWM has been used. Between 20 Hz to 50 Hz optimal PWM is used. Beyond 50 Hz square wave is generated. The multimode system utilizes the advantages of a particular strategy in the given freq range. Apart from this multimode feature, this scheme, which uses a powerful 16 bit CPU (8086), incorporates complex software, giving better frequency resolution.

Some Japanese engineers [10] have gone in for a dedicated LSI chip for PWM generation and other control features, which along with a single chip microcomputer makes a complete system including closed loop control. It has some limitations such as small carrier to output freq. ratio, only SPWM control. This is best suited for thyristor inverters.

Other techniques like DMA control, Bang-Bang control, sine wave approximation etc have been tried. Both 8 bit and 16 bit CPU's have been employed. It has been reported that usually a eight bit CPU is too slow [7] especially for regular SPWM, where multiplication is involved. Hence for increased carrier frequencies, one has to go in for hardware multipliers, which increases the costs by many folds. With the use of 16 bit CPU's like 8086, the availability of multiply and divide

instructions makes the job easier. But since an eight bit manipulation is found satisfactory, μp's like 8088, with 8 bit external data line and 16 bit architecture, could be more suited for such applications. Because of powerful CPU's 16 bit processors, apart from PWM generation, can do a variety of other functions such as, closed loop control, health monitoring, diagnosis and protection etc.

3.1.1 Present Scheme

It was found that the schemes so far implemented, do not mention about the CPU time available for closed loop calculations, after it has attended to the generation of firing pulses. Therefore a need was felt to relieve of the CPU for closed loop calculations, so that a complete system with single CPU would be possible. For economic reasons an 8 bit (8085A) processor was choosen.

The carrier frequency around 2 KHz makes this firing circuit suitable for a power transistor inverter. But at this frequency, the carrier period is around 500 μ sec. In SPWM, one multiplication per phase per carrier cycle is needed. Thus for a 3 ph output, multiplication time itself comes out to be 400 μ sec (approx 130 μ sec/multiplication with 3 MHz clock). Secondly, for a scheme with 1 counter per phase there are 5 interrupts per carrier cycle. Just the PUSH and POP operations

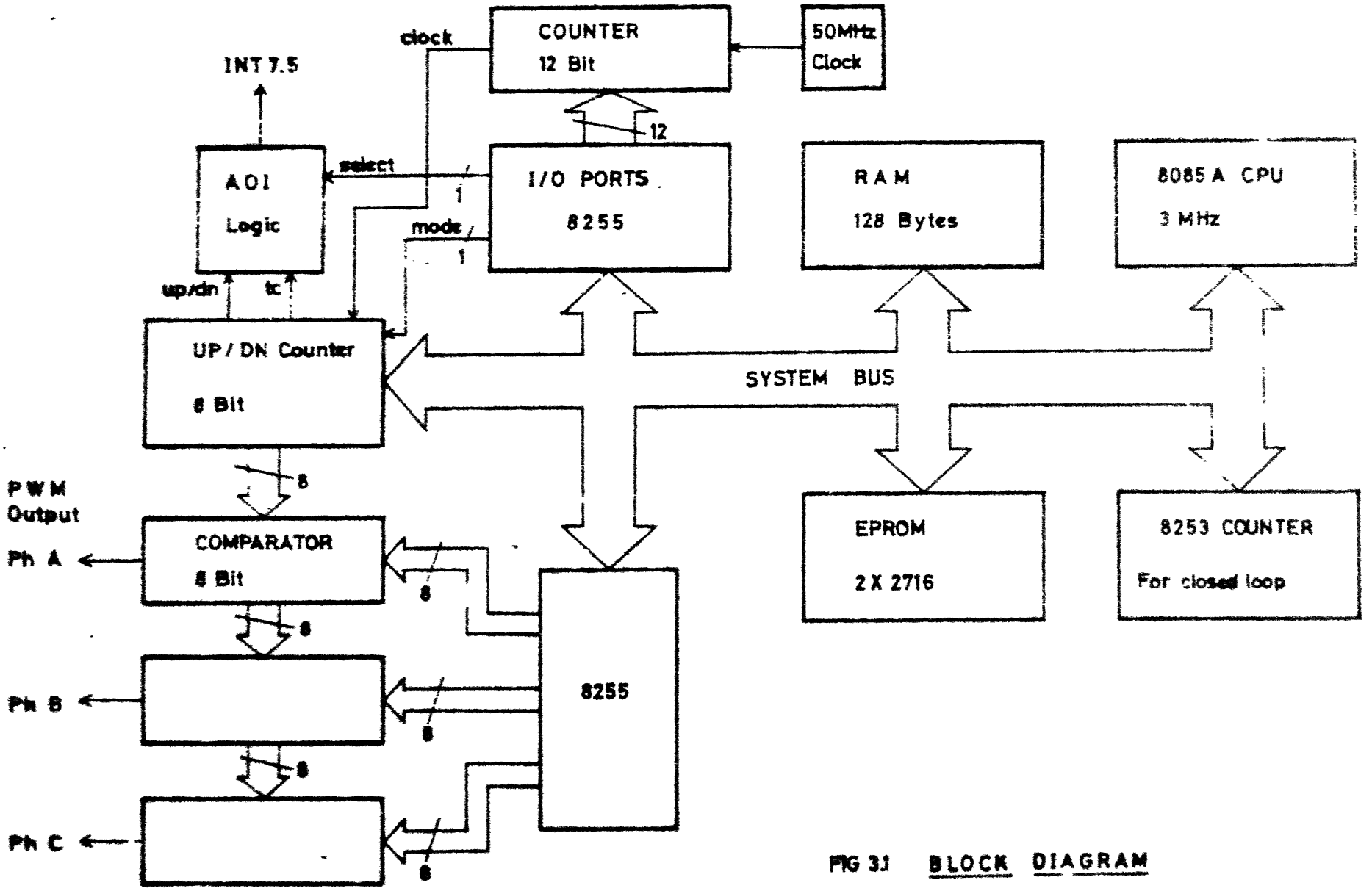


FIG 3.1 BLOCK DIAGRAM

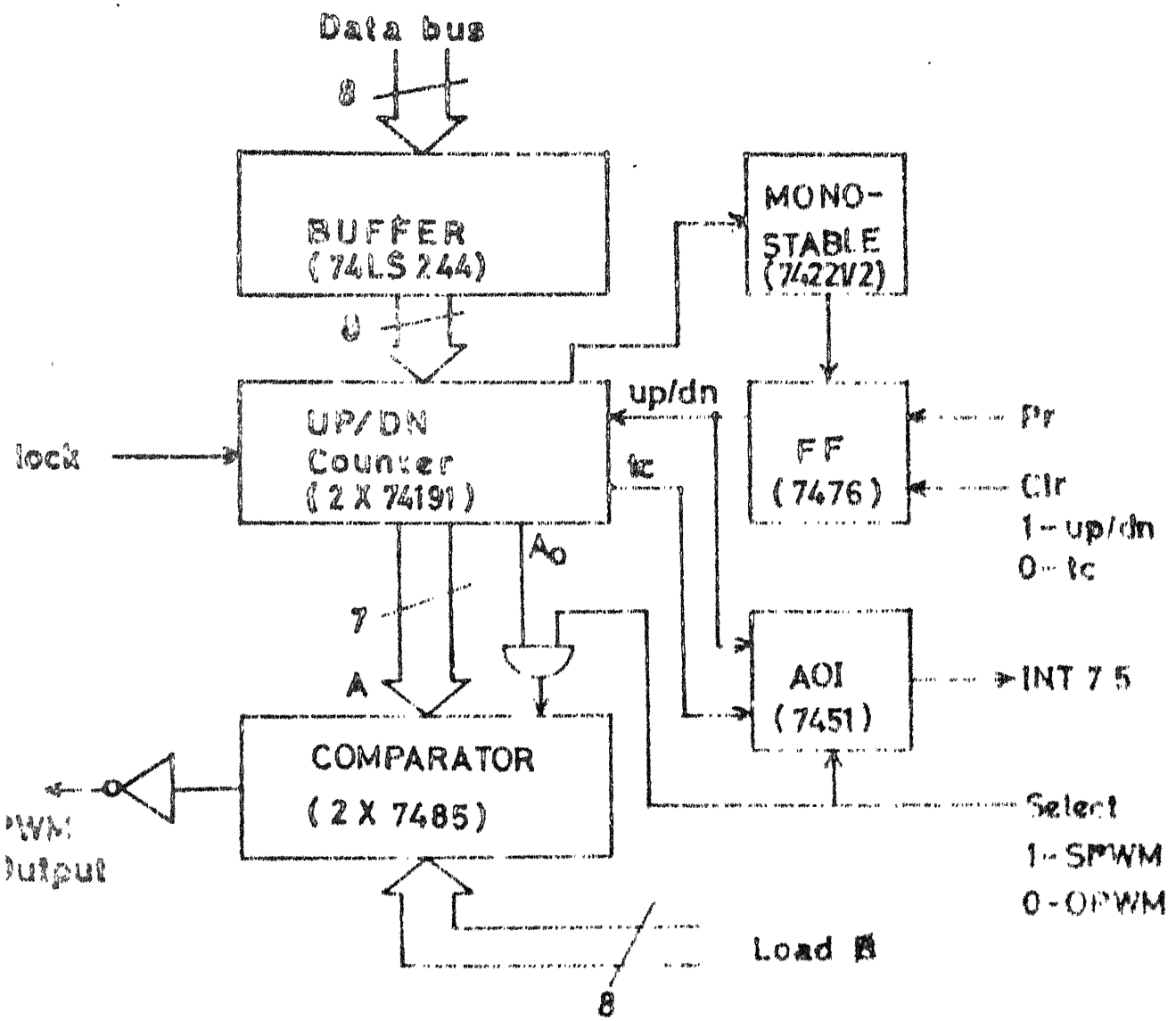


Fig 3.2 PWM WIDTH GENERATION

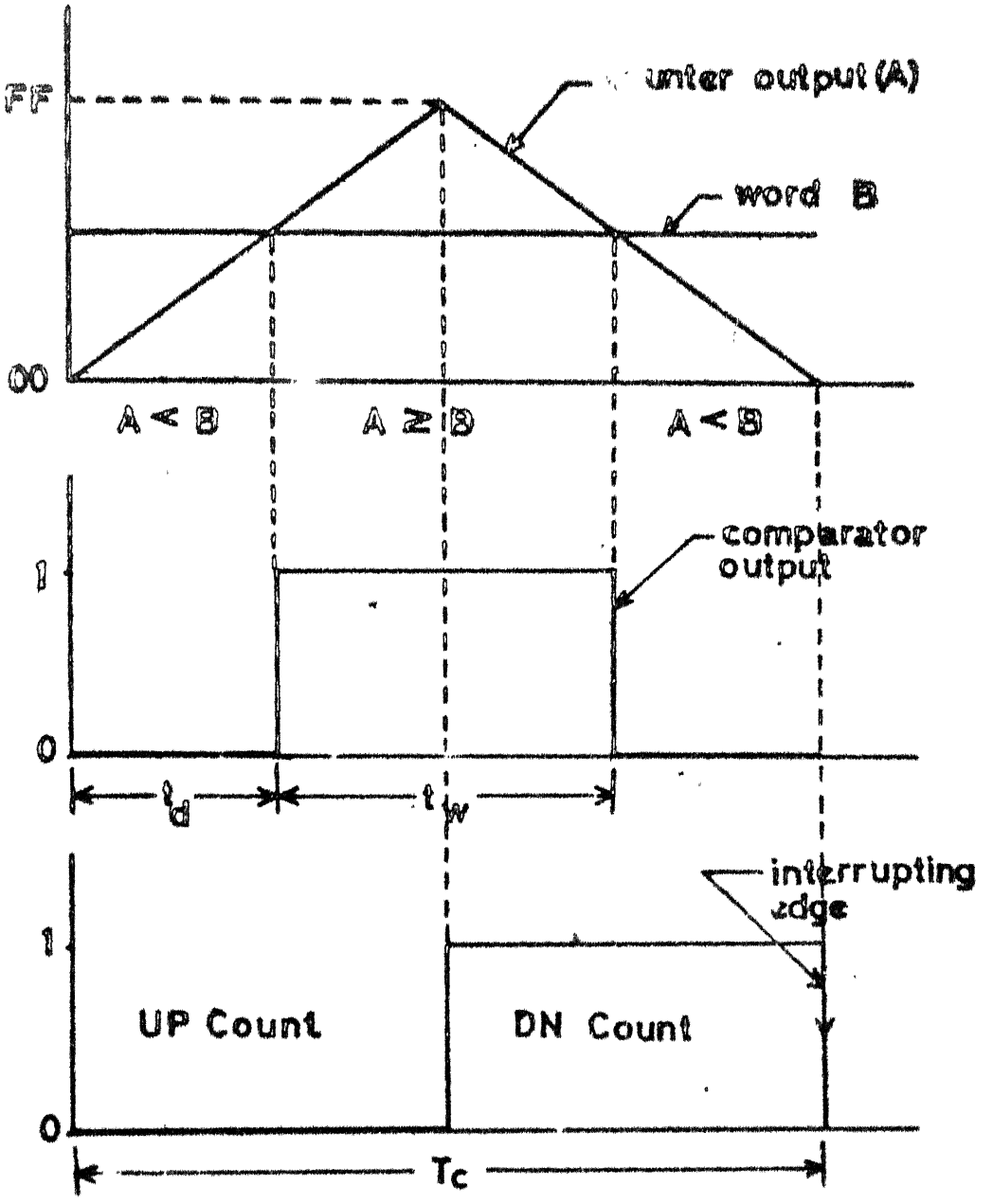


Fig 3.3 DIGITAL COMPARISON

of register pairs waste more than 150 μ sec. But by rewriting a more efficient multiplication algorithm and by reducing the number of interrupts to one percarrier it was possible to implement the firing circuit with frequency ratios as high as 192 and carrier around 2 KHz. To get maximum possible CPU time for closed loop operation all interrupt servive subroutines were optimised as much as possible. The hardware and software involved is discussed in detail in the following sections. The block diagram is shown in fig. 3.1.

3.2 HARDWARE REALISATION

3.2.1. Width Generation with One Interrupt

It is possible to reduce the number of interrupts to one, by doing the comparison, with a hardware comparator, as shown in figs 3.2 and 3.3. An 8 bit UP/DN counter output was fed to the input A of the comparator and an 8 bit port was connected to the B input (Note that the monostable is required to satisfy some conditions of 74191 during mode change, see also the circuit diagram Appendix A).

The comparator pin A < B inverted gives the required output. Thus by loading a word at B proportional to t_d, a width t_w can be generated. The carrier period T_c can be changed by charging the clock to the counter. For 3 ph outputs 3 comparators and 3 ports are needed. The falling edge of the

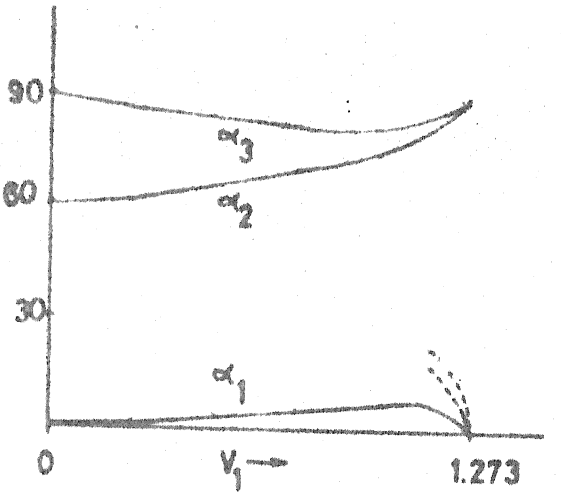


Fig 3.4 OPTIMAL SWITCHING

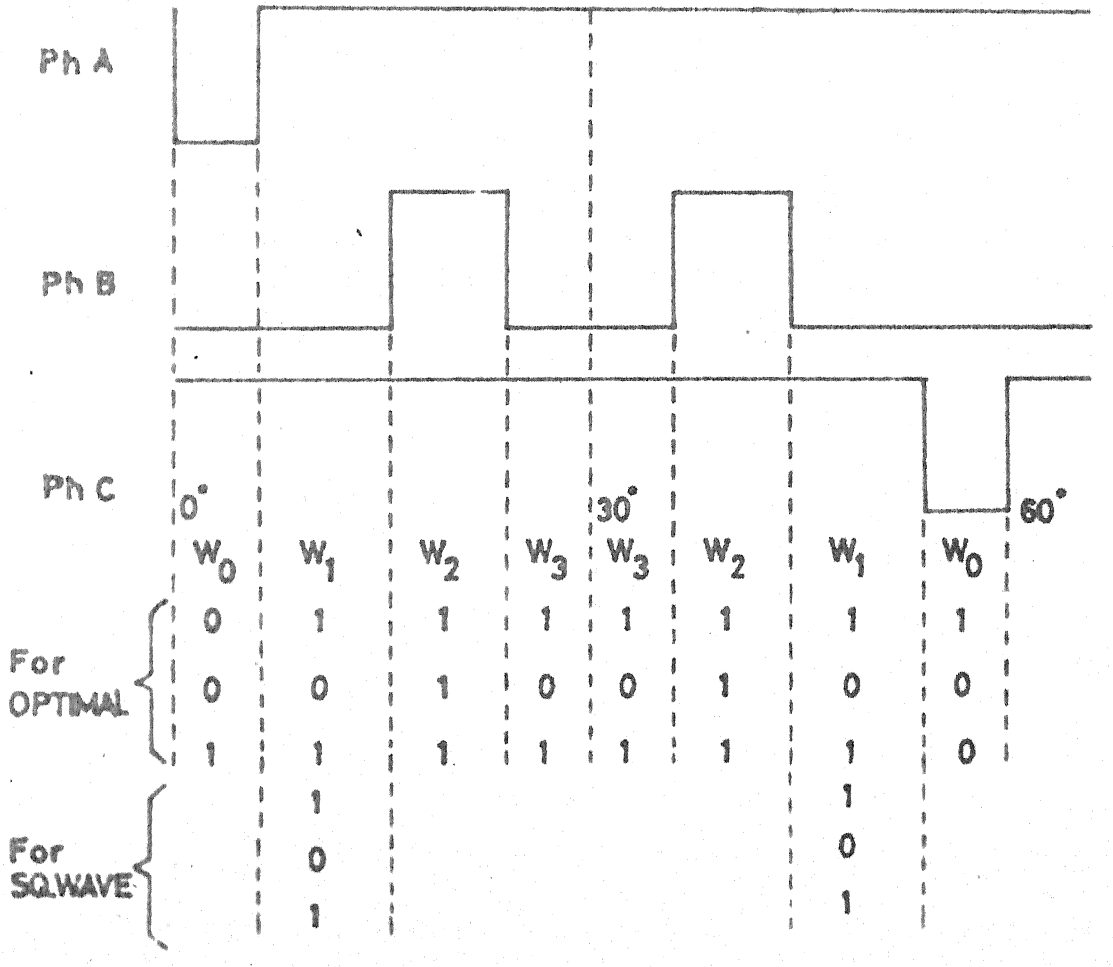


Fig 3.5 OPTIMAL WIDTHS & STATUS

UP/DN output is used to generate interrupts. The interrupt service routine first outputs the widths (proportional to t_d) calculated in the previous cycle and then calculates new widths for next carrier cycle. Even though one carrier cycle delay is involved, it is negligible compared to the motor time constant.

3.2.2 Adoption of Hardware for Optimal PWM

To implement optimal PWM strategy, with all the advantages of reduced CPU time, suitable modifications were made in the hardware. It can be seen from figs 3.4 and 3.5 that, a status information of 3 phases from 0 to 30° interval is sufficient to generate the complete 3 phase wave. Hence an information of widths W_0, W_1, W_2 and W_3 and the status of phases stored for a complete cycle is sufficient to generate a complete wave. Similarly, in this way, the change over to square wave is simple because, square wave is a special case of the optimal switching.

This technique is chosen, since it requires only one counter. The same updown counter is used, by keeping it always in down mode. This can be easily done by making preset of flip flop high and clear low. Now the widths are loaded into the counter, through a burfer, as shown in fig 3.3. The terminal count (t_c) is used as an interrupt to the μp, so that it loads the next width. An AND-OR-INVERT (AOI) gate is used to select either an interrupt on terminal count or interrupt on carrier.

The mode change can be controlled by using bit set reset feature of port C of 8255 I/O port.

To output the status of each phase, the same ports are again utilized, with either OO or FF loaded. When we load OO, the output $\overline{A<B}$ is high. But when FF is loaded, notches are introduced at a point when counter becomes FF (Feature of 7485). To overcome this problem, a gate at the LSB bit of counter output is used to force it always low, so that input A to the comparator does not become FF and the notches are eliminated.

Thus with a little increase in the hardware, it has been made possible to implement a complex PWM multimode strategy in 8085 processor.

3.2.3 Variable Frequency Clock

To change the output frequency, the clock to the counter has to be changed. A digitally controlled clock was obtained by dividing a 50 MHz crystal clock, with a 12 bit counter. A high value of crystal frequency is necessary to generate smallest possible steps in frequency.

For asynchronous SPWM the carrier frequency remains constant, where as the Freq. word for synchronous SPWM has to be calculated for a change in frequency, using the following equation.

$$\text{Freq.word=FW} = \frac{50 \times 10^6}{512 \times n \times f} \qquad (3.1)$$

Where n No of samples/cycle, f output frequency.

For optimal PWM

$$FW' = \frac{50 \times 10^6}{256 \times 12 \times f} - \text{correction due to delay in loading} \qquad (3.2)$$

Division by 12 comes due to the fact that 30° interval is stored as a look up table. A correction has to be applied to the frequency word, because after the interrupt comes, there is some delay due to processing, till the width is loaded into the counter. With the present software it was found to be 24 μ sec. The correction is calculated as follows.

$$\text{Correction} = \frac{\text{delay in } \mu \text{ sec. x No. of interrupts in } 30^\circ}{256 \times \text{crystal clock period in } \mu \text{ sec}} \qquad (3.3)$$

$$= \frac{24 \times 3}{256 \times 0.02} = 14$$

For different number of interrupts the correction is found and applied to FW in those ranges.

The division of 12 bits was sufficient because the frequency word ranged from 50 to 840. Two 74191 and one 74197 were cascaded. 74197 has a clocking frequency of 50 MHz, hence it was put at LSB. Since 74197 is only a UP counter, the

compliment of actual number is loaded, in it. After the terminal count, the number is reloaded into the counter. The monostable was necessary to maintain minimum load pulse width required for 74191. An 8255 port A and port B upper were used to latch the number.

3.2.4 Turn on Delay in the Output

The fact that turn off of a power transistor is much slower than the turn on, requires a delay to be given for the turning on of a transistor in a leg of the inverter. This delay was provided by using monostables, with required delay incorporated by suitable values of R and C. The waveforms are shown in figure 3.6. Any on giving transistor is delayed by a time ΔT.

Other hardware includes, a control line which will force all the outputs to zero is provided which can be used for start/stop and in fault conditions.(See Appendix A). Three control facilities are incorporated, one is a control line from the microcomputer, one switch for user control and a fault line. Any one of them going low will disable the output.

3.3 SOFTWARE

As mentioned earlier, the interrupt service rountines (ISS) are most frequently executed, so as to save maximum possible

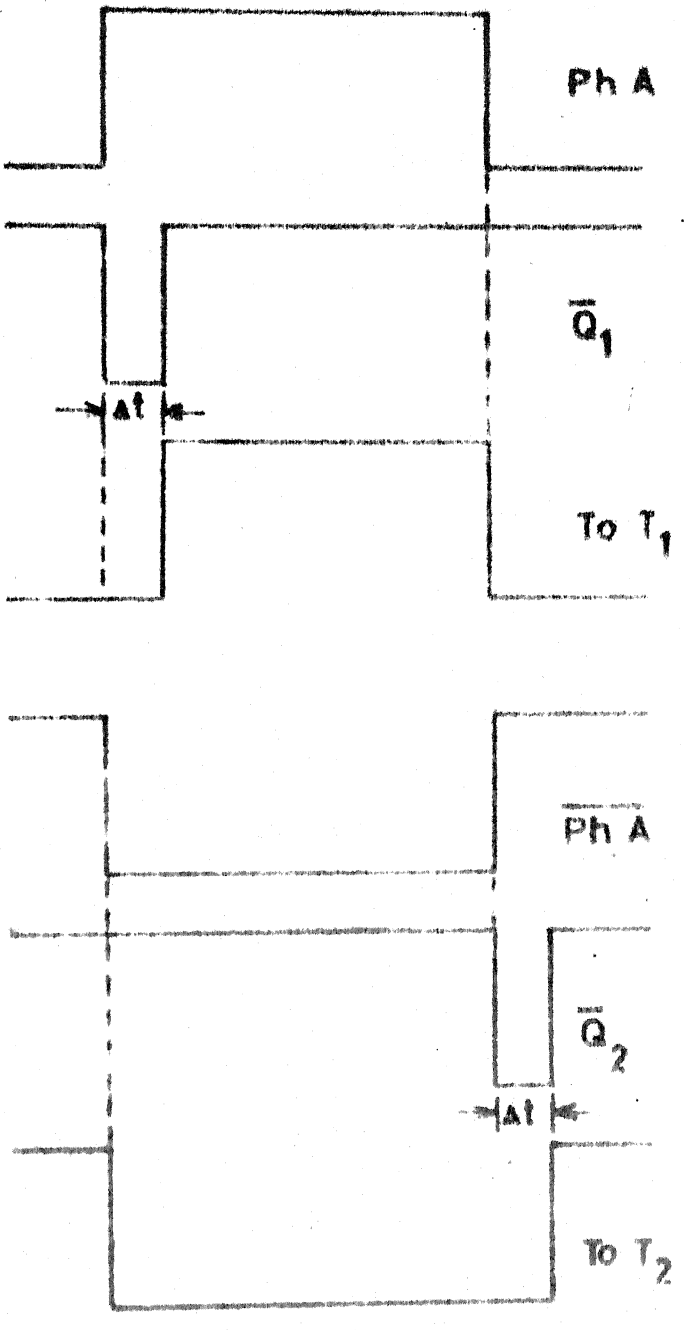


Fig3.6 TURN ON DELAY

CPU time for closed loop and other functions, an efficient ISS is a must. The CPU gives highest priority to ISS. Next comes the mode changing and then the remaining time is utilized for user interaction. When the interrupt comes, present mode is found out and routine jumps to that mode.

3.3.1 The flow charts and their explaination, for each mode is given here. The assembly language programs with list file is given in appendix B.

I) Synchronous SPWM (MODE 1) :

The expression for pulse width is given by

$$W = 0.5\ N\ [\ \frac{V_S}{V_{SM}}\ \text{Sin}\ \Theta + 1]\ \text{for}\ \ 0 \leqslant \frac{V_S}{V_{SM}} \leqslant 1 \qquad (3.4)$$

where V_S/V_{SM} is the ratio of output voltage to maximum output voltage.

Therefore W_d proportional to t_d (fix 3.2) is

$$W_d = 0.5\ (N - W)$$
$$= 0.25N\ [\ 1 - \frac{V_S}{V_{SM}}\ \text{Sin}\ \Theta\ ] \qquad (3.5)$$

With N = 512, M Modulation index 8 bit resolution (V_S/V_{SM}) and $\emptyset$ = Sin Θ with 7 bit magnitude and 1 bit sign.

$$\therefore W_d = 0.25 \times 512\ [127 \times 255 - M.\ \emptyset]\ \frac{1}{127} \times \frac{1}{255}$$

$$\approx \frac{32385 - M.\ \emptyset}{256} \qquad (3.6)$$

This approximation gives an error of 3 at W_d = FF. When W_d = OO, there is no error present. To even out this error 1.5 x 256 = 384 is added to 32385

$$\therefore W_d = \frac{32769 - M.\,\emptyset}{256} = \frac{8001H - M.\,\emptyset}{0100H} \qquad (3.7)$$

The flow chart for mode O is given in figure 3.7.

II) Asynchronous SPWM (MODE O) :

In asynchronous SPWM, the carrier frequency remains constant. The change in output frequency is brought by changing the number of carrier cycles per sample. Here with 192 samples of sine values stored, at 0.5 Hz there are 20 carriers per sample and at 5 Hz there are 2 carriers per sample.

This was implemented in software. A word Y' is calculated as

$$Y' = \frac{f_c \times 512}{f \times n} \qquad (3.8)$$

f_c = carrier freq. f = output freq. n = no of samples/cycle.

It indicates number of carriers per sample x 512. For a given output frequency, for every pulse width generated, a number 512 is subtracted. The remaining value of Y if less than 512, the pointers are updated and Y' is added to the difference. This process is indicated in the flow chart fig 3.8.

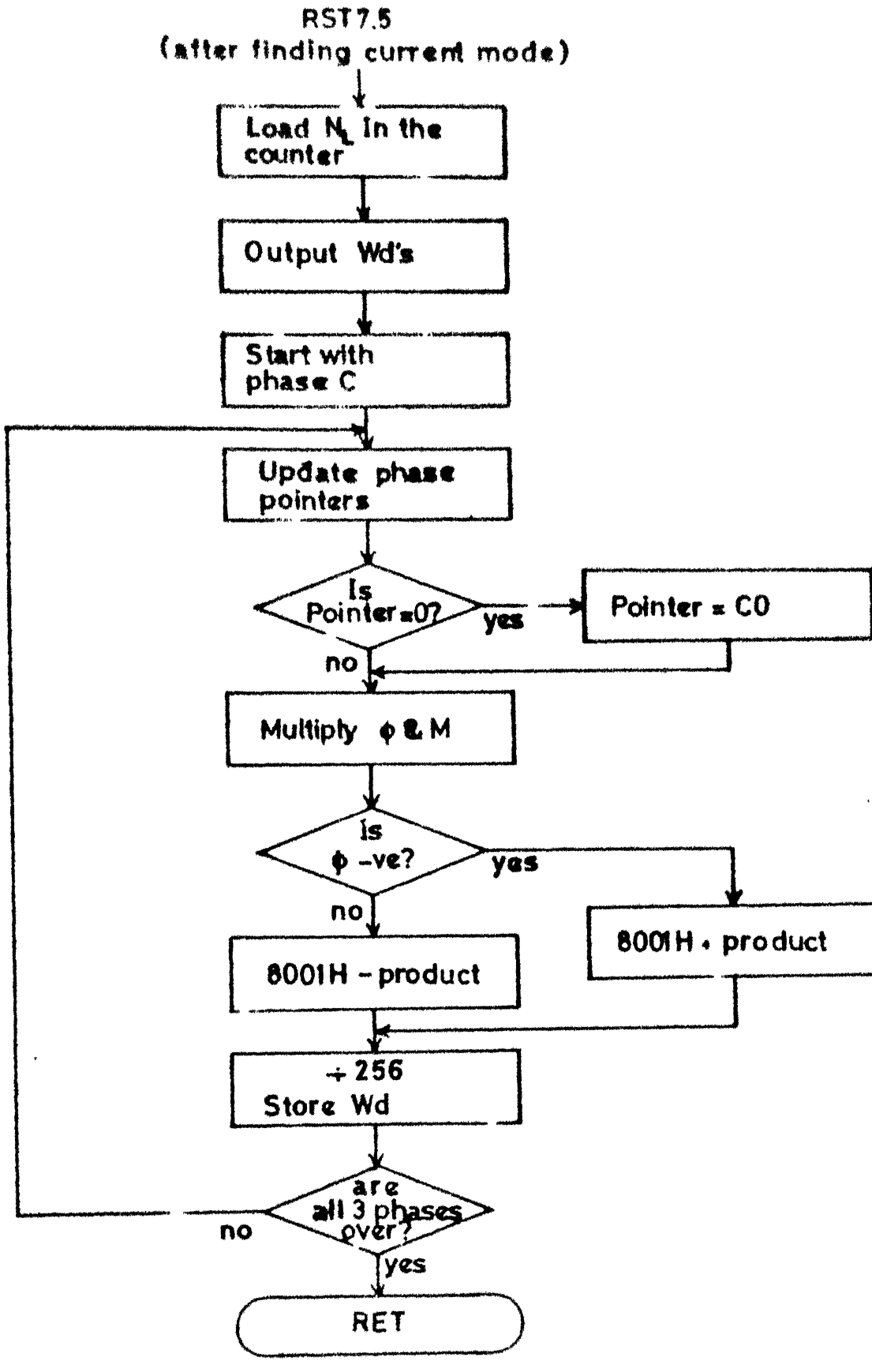


Fig 37 SYNC SPWM 1 (MODE 1)

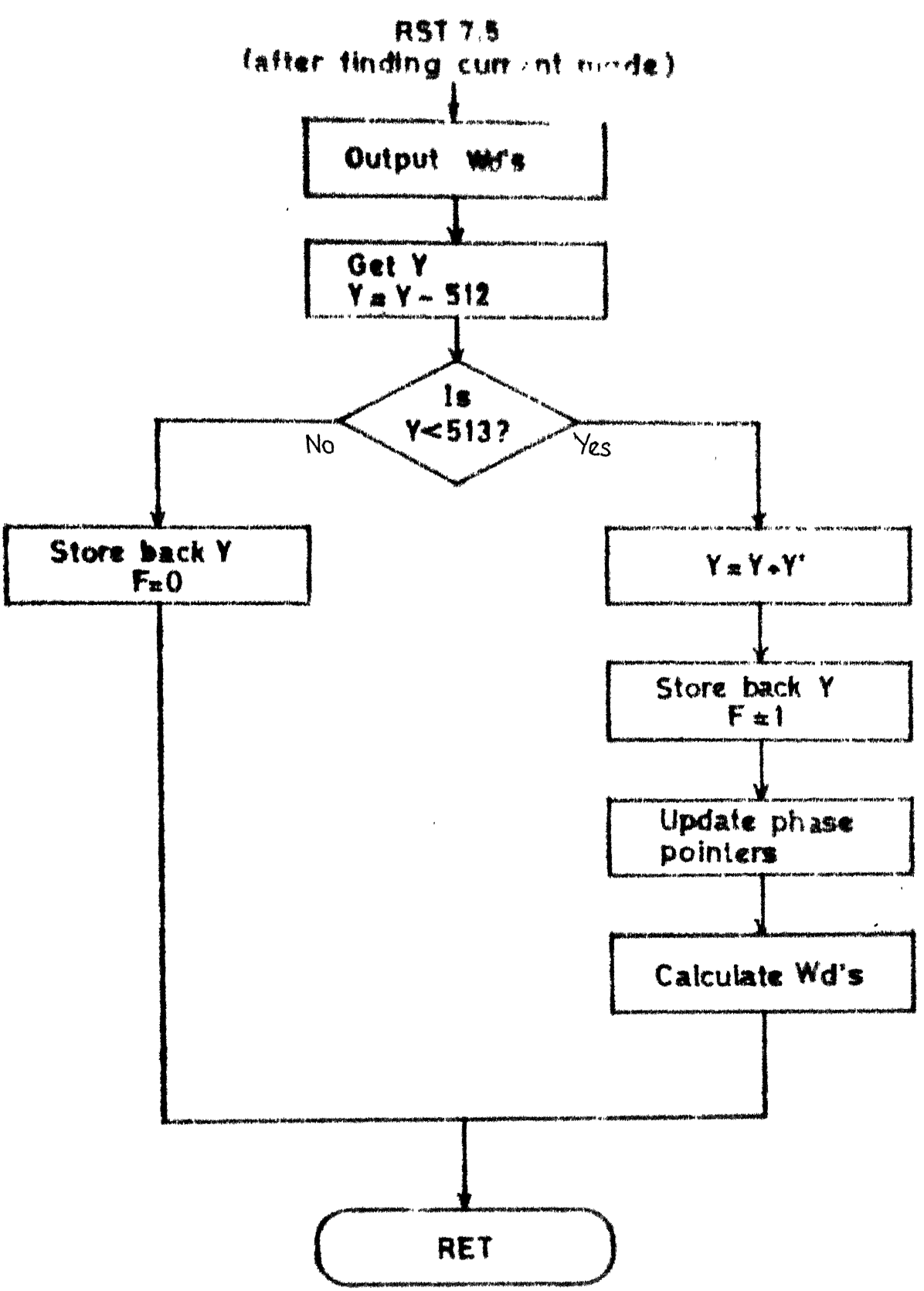


Fig 3.8 ISS FOR ASYNC SPWM (MODE 0)

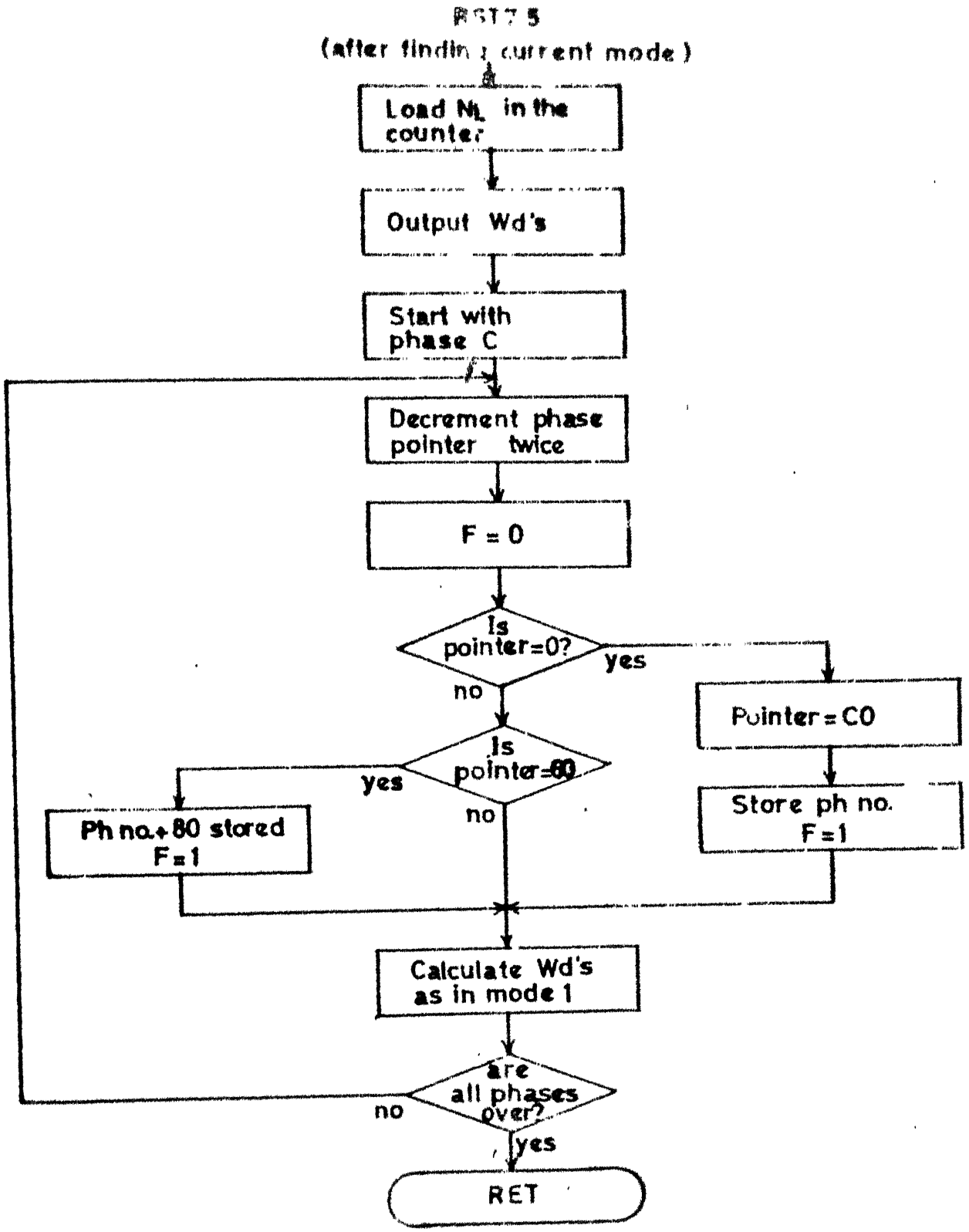


Fig 3.9 SYNC SPWM 2 (MODE 2)

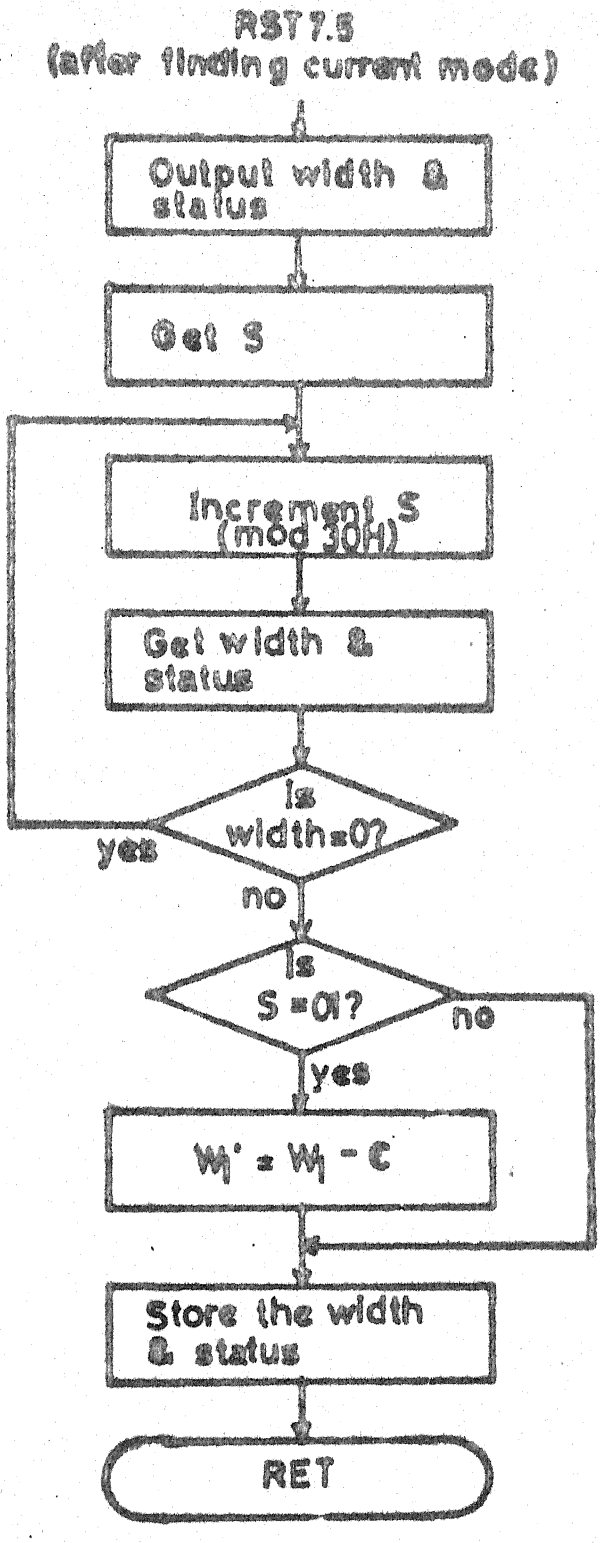


Fig 3.10 OPTIMAL PWM (MODE 3).

This process introduces an error in the frequency, which can be as large as one carrier per cycle. This error is maximum at highest values of frequency in ASPWM mode. Near 5.5 Hz, the number of carriers per cycle is 349. Therefore the maximum error will be 0.014 Hz.

III) Synchronous SPWM 2 (MODE 2):

This mode is the same as mode 1 with a freq ratio of 96, hence the phase pointers are updated twice, thus utilizing every alternate sample of sine table. This mode needs slight modification, to facilitate mode changing. From synchronous SPWM, the mode can charge to optimal, hence suitable changes were made which are indicated in the flow chart (fig 3.9).

IV) Optimal PWM (MODE 3):

The optimal PWM was implemented, by storing the widths in a look up table, with a voltage jump of 0.39 %. The LSB address of the look up table is formed by the modulation index. The MSB address is decided depending upon the instant at which the cycle is. For one complete cycle, for the given optimal switching with 3 switching per quarter cycle, there are 48 status of the 3 phases. These were also stored in a table. For a given instant, the status of each phase was read and appropriate words either 00 or FF were loaded in the ports.

Nearer to 50 Hz, the number of switchings were gradually decreased, this is done by checking if the width is zero (fig 3.10). If it is zero, the next status number was taken. Thus in square wave only 12 out of 48 status are outputted per cycle.

3.3.2 Frequency Resolution Improvement

The scheme as it is, would give poor frequency resolution, especially nearer 10 Hz and 20 Hz in synchronous SPWM and at higher values of frequencies in optimal. The reason being, at these values, step change in clock is too large.

The output frequency will always be higher than the specified frequency due to round off errors in FW calculation. To overcome this difficulty, following schemes have been implemented.

In synchronous SPWM, the contents of the UP/DN counter are altered, so that carrier period increases in proportion to the correction needed in the frequency.

No. to be loaded in the counter = Counter value at the time of loading − Correction per carrier

or

$$N_L = N_C - C \qquad (3.9)$$

N_C can be found out by knowing the time delay in loading the counter after the interrupt has come. This delay, with the present ISS is 32 μ sec.

Therefore it can be easily seen that the equation for N_C in this case becomes

$$N_C = \frac{1600}{FW} \qquad (3.10)$$

The correction can be calculated as follows

$$C = \frac{\left(\frac{1}{f} - \frac{1}{f1} \right)}{n \times \text{clock period}} \qquad (3.11)$$

Where f' is the frequency without any correction. Using equation 3.1, and substituting appropriate values of n, the expression 3.9 simplifies to

For SPWM 1

$$N_L = \frac{1600}{FW} - \left[\frac{508.6 - f \times FW}{f} \right] \times \frac{512}{FW} \qquad (3.12)$$

Similarly for SPWM 2

$$N_L = \frac{1600}{FW} - \left[\frac{1017.3 - f \times FW}{f} \right] \times \frac{512}{FW} \qquad (3.13)$$

The corrections take place in every carrier cycle. At 10 Hz, a minimum of 192 μ sec (clock = 1 MHz), change can be brought about in one cycle of output. This gives the frequency resolution of 0.019 Hz. Similarly in SPWM 2 at 20 Hz resolution is 0.038 Hz.

In optimal PWM, width W_1 (see fig 3.5) is corrected once in each cycle. A lower frequency than the command frequency is generated by incrementing FW. Now the correction can be subtracted from W_1 so as to increase the frequency to the required value. This procedure is necessary, because W_1 equals FF in square wave region.

With similar arguments, the expression in this case becomes

$$W_1' = W_1 \left[\frac{-16340 + f \times FW}{f} \right] \frac{3060}{FW'} \qquad (3.14)$$

At 100 Hz, with a clock of 3.25 μ sec, the resolution works out to be 0.032 Hz.

3.3.3 Look up Tables

I) Sine table :

Sine values were stored in sign magnitude form, with 7 bits magnitude and the MSB sign bit. 192 samples for one complete cycle were stored in a reverse order as shown in fig. 3.11. This reduces comparison times, since the pointers are decremented and are checked whether they are zero or not. Three phase pointers were initialized to 40, 80, C0 for phases C, B and A respectively.

II) Optimal switching table :

For 3 switchings per quarter cycle, widths W_0 to W_3 were stored with 0.39 voltage jump ie 256 steps in 0 to 50 Hz range.

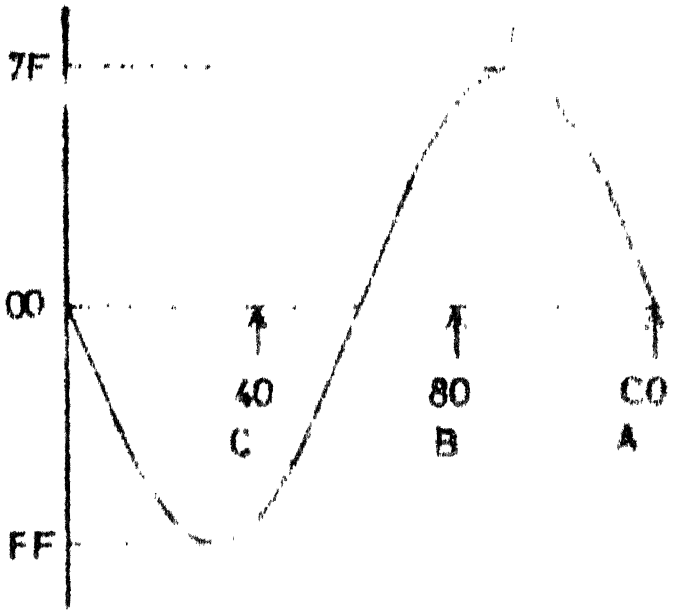


Fig 3.11 SINE TABLE

But since the optimal PWM starts only after 19.5 Hz, the earlier switchings need not be stored. The widths can be found from the following relations.

$$W_0 \alpha \alpha_1$$

$$W_1 \alpha \alpha_2 - \alpha_1$$

$$W_2 \alpha \alpha_3 - \alpha_2$$

$$W_3 \alpha 30^\circ - \alpha_3$$

Widths were stored with 8 bit resolution. Nearer to 50 Hz, the number of switchings were gradually reduced, ultimately making it a square wave, at 50 Hz. The ISS takes 160 μ sec, therefore widths smaller than this value were eliminated, by reducing number of switchings. The switching angles are indicated in table 4.1.

III) Voltage frequency table :

A simple voltage to freq. law, which takes into account the stator resistance of the motor is given by

$$V = R_{1dc} I_r + (V_r - R_{1dc} I_r). \frac{f}{f_b}$$

where

I_r Rated current

f_b Base frequency

V_r Rated voltage

Substituting the various quantities.

$$V = R\ 6.67 \times 2.5 + (220 - 6.67 \times 2.5)\ \frac{f}{50}$$

$$= 16.67 + 4.06.f$$

This was stored in 256 steps, with 8 bits resolution. From the frequency command, the required voltage is found from this table.

3.3.4 Optimization of CPU Time

All possible techniques were used to optimize the CPU time so that the possibility of doing close loop calculations becomes a reality, in a 8 bit CPU. Following are some of the main points.

1. Memory mapped ports reduce comparison times while outputting widths to appropriate ports, since the outputting can be done using register addressing.

2. The multiplication if written in its normal way, needs 48 clock cycles per bit of multiplier. But if written in expanded form (see appendix B) needs 34 clock cycles. Thus it was possible to reduce the multiplication time by 33 %, with little increase in memory requirement. This is the main factor, which has made this firing circuit feasible, in 8085.

3. Sine table was stored in reverse order (fig. 3.11) which will reduce comparison times. Also complete cycle stored reduces software overheads.

4. In this scheme only width t_d is needed to be calculated, which reduces calculation times, unlike in other schemes where both t_d and t_w have to be calculated.

5. The addresses of ISS routines were chosen such that the logic is simplified. Similarly the addresses of various quantities to be stored in RAM were chosen carefully.

6. Those routines which decide the accuracy of the output signal have been optimised to large extent and all possible manipulations have been transferred to other routines.

3.3.5 Mode Changing

The mode changing should occur at appropriate instants. If the frequency lies on the border of two modes, then with small changes in frequency unnecessarily many mode changes would occurs. To avoid this difficulty a schmittriger type characteristic with . over lap of 1 Hz was implemented as shown in figure 3.12.

All the parameters of a particular mode were changed, only after disabling the interrupt.

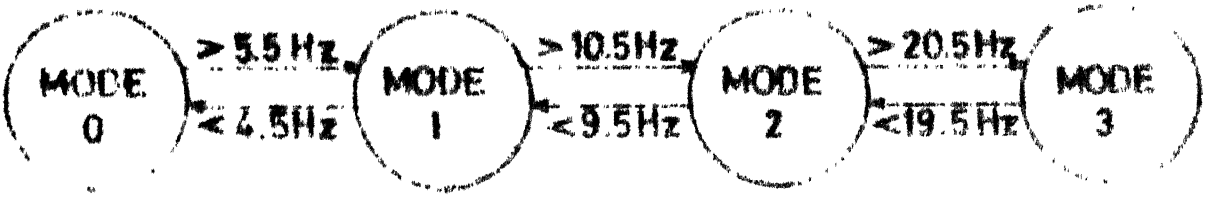


Fig 3.12 MODE CHANGING

I) Mode changing between Mode 0 and Mode 1:

While mode is being changed from mode 0 to mode 1, the flag F (fig 3.8) is checked and wherever it is 1, mode change is effected so that charge occure only at next sample. Frequency word and mode number are also changed.

To change from mode 1 to mode 0, value of Y' is calculated and loaded. The frequency word is also changed.

II) Mode changing between Mode 1 and Mode 2 :

Mode change from mode 1 to mode 2 takes place with change in frequency word and making the phase pointers even.

Mode change from Mode 2 to mode 1 takes place without any change except frequency word.

III) Mode changing between Mode 2 and Mode 3 :

To change from Mode 2 to Mode 3 flag F (fig 3.9) is monitored. It is 1 for the duration any phase pointer is at C0 or 60. The phase number indicates the phase which is at C0 or 60. The MSB bit of phase number if 1, indicates it is at 60. The following table stored in memory gives the status number for optimal PWM. The change occurs at the end of any 60°interval.

Phase number	MSB Bit of Ph No.	Status Number
0 (ph A)	0	00H
0 (ph A)	1	18H
1 (ph B)	0	10H
1 (ph B)	1	28H
2 (ph C)	0	20H
2 (ph C)	1	08H

Also the PC_0 line is made high, so as to make the counter in down mode, with interrupt on terminal count.

While changing the mode from 3 to 2, the phase pointers have to be determined depending on the status number. The following table gives the corresponding phase pointers.

Status No.	Phase pointers		
	ph A	ph B	ph C
00	C0	80	40
18	60	20	A0
10	40	C0	80
28	A0	60	20
20	80	40	C0
08	20	A0	60

The mode changing occurs only at the end of any 60° interval.

3.3.6 Initialization and User Interaction

After having attended to the essential needs of the firing circuit, the rest of the CPU time can be utilized for user interaction. Here a facility to choose any desired frequency and mode in an interactive way. was given. The indication of existing mode, freq and percentage modulation was provided. An error message, if the freq goes toohigh or the jump is too high is given. The flow chart for this routine is shown in figure 3.13.

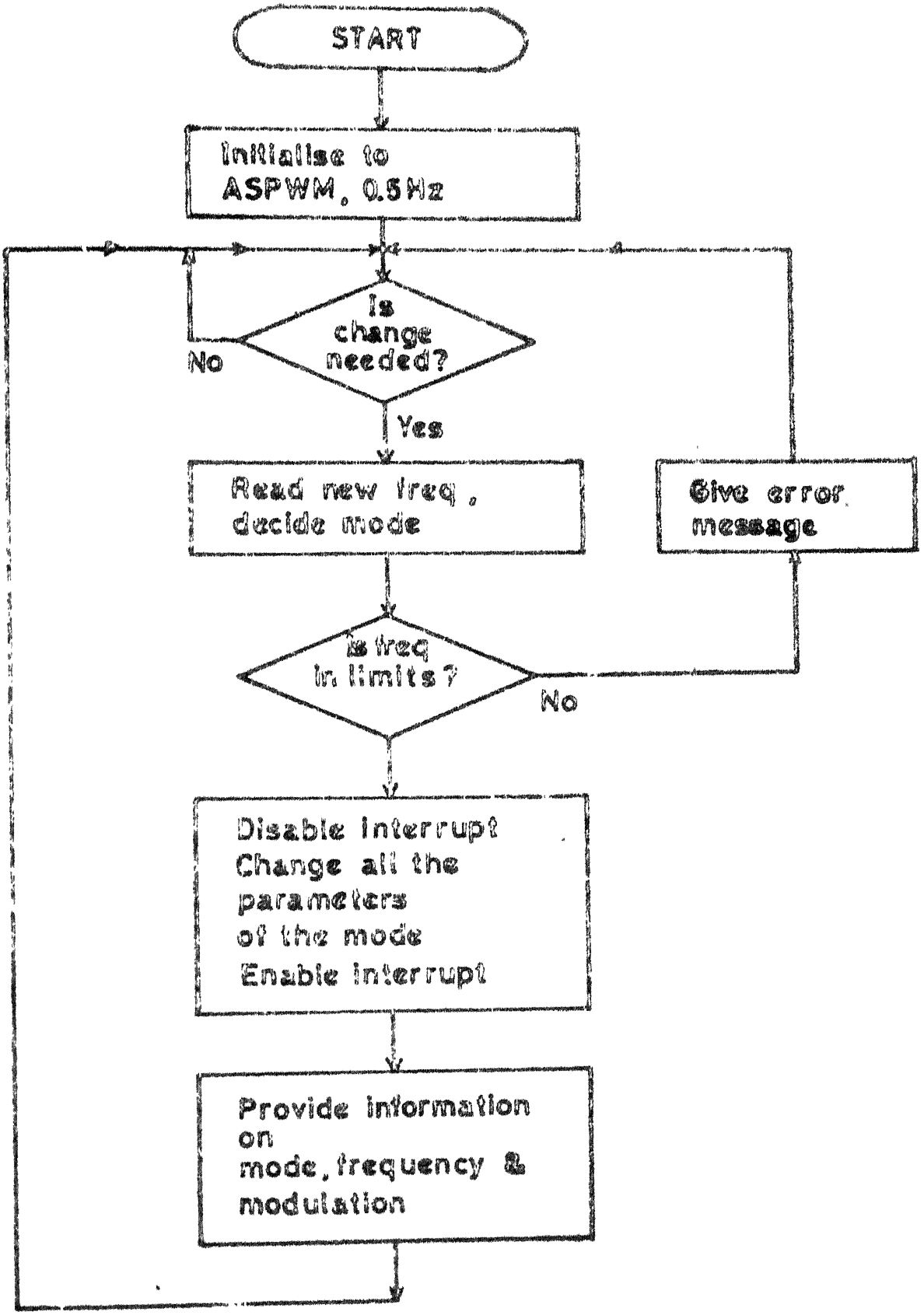


Fig 318 BACKGROUND ROUTINE

3.4 FEATURES AND RERFORMANCE

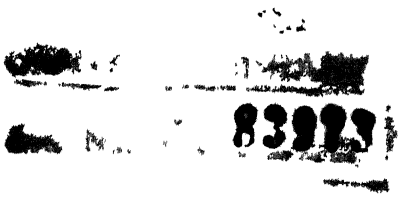
The firing circuit thus implemented has a frequency range from 0.5 Hz to 100 Hz. The frequency resolution is better than 0.038, throughout this range. The voltage step is less than 0.5%. The angle resolution in optimal PWM is 0.12^{o}. In SPWM, the delay in the response (of freq) equals one carrier cycle or maximum of 1 m sec. In ASPWM it is as high as 10 mSec at 0.5 Hz. In optimal PWM, the charge takes place at every 30^{o} thus introducing a max delay of 4.25 m sec at 19.5 Hz. In SPWM, the widths are generated with one interrupt only, hence errors due to ISS delays are not present in the output widths.

It is possible to implement the closed loop control functions in the same CPU. For this purpose the worst case CPU time availability is given in the following table.

Mode	Frequency Hz	Max ISS execution time (μ sec)	Average CPU time available(μ sec) per m sec.
0	5.5	480	420
1	10.5	360	275
2	20.5	380	250
3	43	160	685
3	100	270	675

3.4.1 Further Improvements

The frequency resolution in SPWM can be easily increased by correcting the counter in say alternate carrier cycles or after every 4 carrier cycles etc. Thus frequency resolution can be easily improved to a large extent in SPWM.



CHAPTER 4

SIMULATION OF PWM WAVEFORMS

4.1 INTRODUCTION

Simulation of PWM waveforms is reported keeping in view two points. (1) To study harmonic contents of different strategies and verify the experimental results. (2) To modify the switching instants in the optimal PWM so as to make it suitable for microcomputer implementation.

The method of simulation as proposed by S.R. Bowes and R.R. Clements [14] has been adopted. It readily provides a modelling technique for PWM waveforms such as natural SPWM, regular SPWM, optimal PWM etc. Single as well as three- phases can be simulated for determining harmonic components and content using this modelling technique.

4.2 COMPUTER SIMULATION OF PWM SYSTEMS

The most general pulsed periodic waveform can be represented as

$$y(\phi) = y_1 \{ H(\phi) - H(\phi-\alpha_1) \} + \sum_{j=2}^{n} y_i \{ H(\phi-\alpha_{j-1}) - H(\phi - \alpha_j) \}$$

$$+ y_1 \{ H(\phi - \alpha_n) - H(\phi - 2\pi) \} \text{ for } 0 \leq \phi \leq 2\pi$$

and $y(\phi) = y(\phi \bmod 2\pi) \qquad \phi < 0 , \phi > 2\pi$

Where $H(\emptyset)$ is the heaviside unit function. The waveforms have n switching points α_1, α_2, α_3 --- α_n between each pair of which the waveform has a fixed constant level, represented by y_1, y_2--- y_n respectively. Such a waveform can be represented by 2n+1 parameters, the number of switching points n, and two vectors of α and y.

4.2.1 Regular Sampled PWM

The equation for the pulse width (in radiams) for a single phase PWM waveform (fig. 4.1) with a frequency ratio R and modulation index M is given by

$$\alpha_w = \frac{\pi}{R}\{ 1 + M \sin (2j - 1) \frac{\pi}{R} \} \quad \text{where } j=1,2, \text{ --R.}$$

Transition from - 1 to + 1 occurs at (sec fig 4.1)

$$\alpha_{2j-1} = (2j - 1) \frac{\pi}{R} - \frac{\alpha_w}{2}$$

$$= (2j-1) \frac{\pi}{R} - \frac{\pi}{2R} \{ 1 + M \sin (2j-1) \frac{\pi}{R} \}$$

$$= \frac{\pi}{2R} \{ 4j-3- M \sin (2j-1) \frac{\pi}{R} \}$$

Similarly transition from +1 to -1 occurs at

$$\alpha_{2j} = (2j-1) \frac{\pi}{R} + \frac{\pi}{2R} \{ 1+ M \sin (2j-1) \frac{\pi}{R} \}$$

$$= \frac{\pi}{2R} \{ 4j-1+M (2j-1) \frac{\pi}{R} \}$$

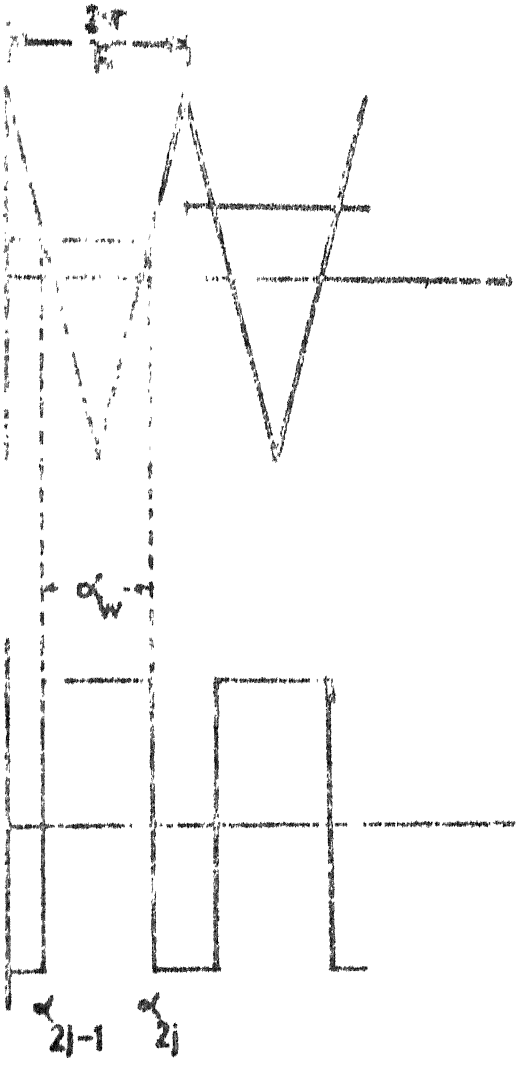


FIG 4.1

And the levels are given by

$$\left.\begin{aligned} y_{2j-1} &= -1 \\ y_{2j} &= +1 \end{aligned}\right\} J = 1,2, \text{ -- } R$$

The switching instants and levels thus found are stored as vectors which are then further processed.

4.2.2 Asynchronous SPWM Waveforms

To get asynchronous SPWM waveform, first the regular PWM waveform of required frequency ratio and modulation index is generated. According to the number of carrier cycles involved in one sample that many multiple pulses are generated and then the complete cycle is adjusted within 2π.

4.2.3 Optimal PWM Waveform

The optimum switching instants are directly fed through the keyboard. Due to quarter wave symmetry only instants up to $\pi/2$ are to be fed. The complete waveform up to 2π is then generated by simple differencing.

The square wave is only a special case of optimised PWM and can be studied by feeding appropriate switching instants.

4.3 PROCESSING OF WAVEFORM

After having generated the PWM waveform it is necessary to process it so as to generate a 3 phase waveform, in addition,

to incorporate the various practical limitations of switching components.

The conversion to 3 phase is done, by generation and another phase with 120° phase difference. Then the differencing is done to get the actual line voltages. A two level single phase waveform gives rise to a 3 level 3 phase waveform. Any other practical considerations could be incorporated, such as the quantization errors involved in the microcomputer implementation.

4.4 HARMONIC ANALYSIS

The model obtained in section 4.2 can be easily employed for harmonic analysis, in which the frequency domain analysis is carried out. The maximum number of harmonics of interest can be studied. Also the summation of individual components can be done to get an over all harmonic content of the waveform.

The Fourier breakdown of one of the component pulses of a period is given by

$$H(\phi - \alpha_{j-1}) - H(\phi - \alpha_j) = \frac{\alpha_j - \alpha_{j-1}}{2\pi}$$

$$+ \sum_{m=1}^{\infty} \frac{1}{m\pi} \{(\sin m\alpha_j - \sin m\alpha_{j-1})\cos m\phi - (\cos m\alpha_j - \cos m\alpha_{j-1}) \sin m\phi \}$$

Which yields the Fourier coefficients as follows.

$$a_m = \frac{1}{m\pi}\left[y_1(\text{Sin } m\alpha_1 - \text{Sin } m\alpha_n) + \sum_{j=2}^{n} y_i(\text{Sin } m\alpha_j - \text{Sin } m\alpha_{j-1})\right]$$

$$b_m = \frac{-1}{m\pi}\left[y_1(\text{Cos } m\alpha_1 - \text{Cos } m\alpha_n) + \sum_{j=2}^{n} y_i(\text{Cos } m\alpha_j - \text{Cos } m\alpha_{j-1})\right]$$

From which the Fourier coefficients of the harmonic series is found. Which helps calculating the amplitudes of all the harmonics. The total harmonic contents in the current waveform of the simulated wave, by specifying the required load can be found.

4.5 RESULTS AND DISCUSSION

To simplify the comparison of results the term percentage modulation has been used. 100% modulation corresponds to square wave output or $V_1 = 4/\pi$. For a modulation index of 1 in SPWM or $V_1 = 1$ in optimal the percentage modulation is 78.5. The y axis of the graphs indicates the amplitude in rms per unit of dc link voltage.

Figs 4.2 (a) to (g) show the harmonic spectra of synchronous SPWM, with frequency ratios of 48, 96 and 192. In all these the prominent harmonic is the carrier wave. A comparison of spectrum for a particular frequency ratio and for different modulation indices show that with a reduction in the

modulation index the amplitude of the carrier increases. Fig. 4.3 (a) to (g) indicate the spectrum for 3 phase SPWM waveforms. The carrier in all these waveforms is absent because it is a multiple of 3. Fig. 4.4 (a) and (b) show asynchronous SPWM with two carriers per sample for percentage modulation of 70.7 and 5.54 respectively. At 5.54 modulation, the harmonics near the carrier become insignificant.

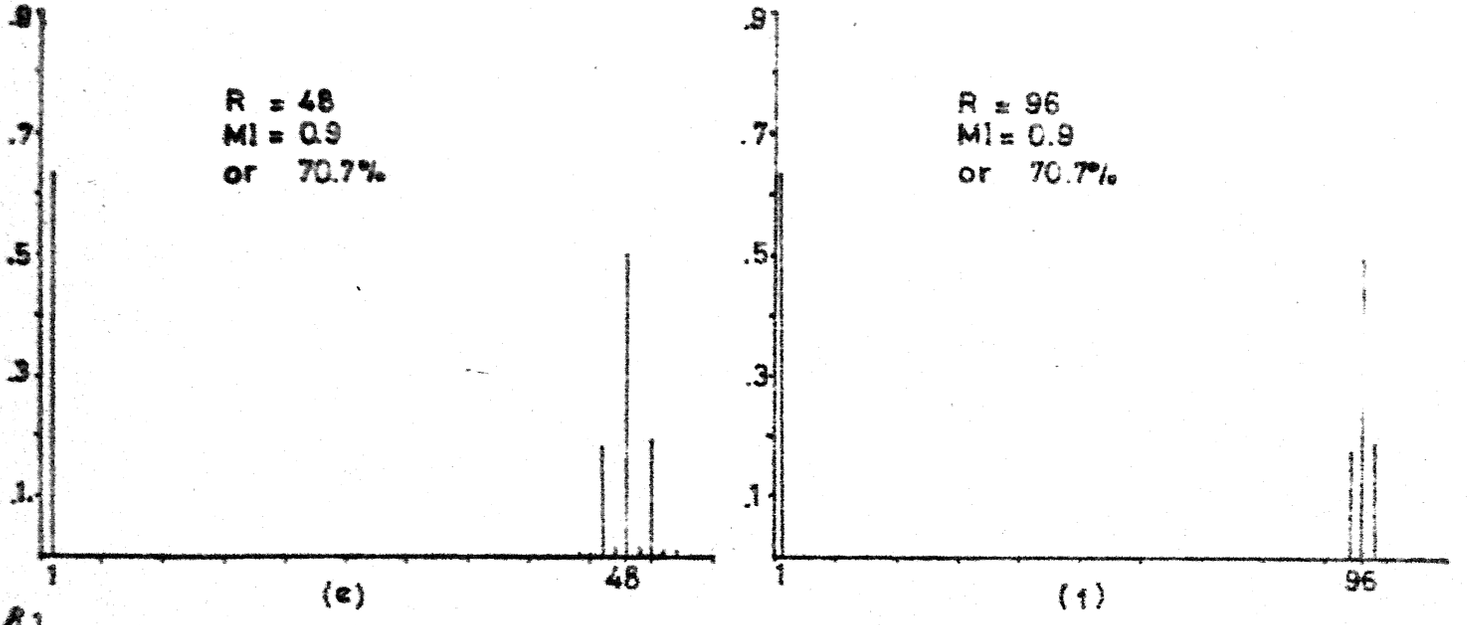
Figs 4.5 and 4.6 show the harmonic content of an optimal PWM waveform with different modulations for single-phase and three-phase respectively. In the three phase, the triplen harmonics are absent.

To make the microcomputer implementation feasible in the frequency range of 43 Hz to 50 Hz. The number of switchings were gradually reduced. An attempt is made to maintain linear variation of fundamental within permissible limits of $\pm$ 5%. Fig 4.7 shows the extreme limits of amplitude variation with either $\alpha_3 = 90^\circ$ or $\alpha_2 = \alpha_3$. Using these as guide lines proper switching instants are found out by trial and error method. Modified switching angles are given in Table 4.1. The harmonic content over this frequency range is also obtained. Fig. 4.8 shows the comparison of harmonic currents for global minima, local minima and reduced number of switchings.

To obtain the total harmonic current, for a given RL load, the harmonic components are summed. The variation of the total harmonic content, and the fundamental current, with the output frequency are illustrated in 4.9. The harmonic content in SPWM is low. In optimal, the harmonic content is high, but gradually reduces with frequency. In the frequency range of 42 to 48, the increase in the harmonic content, results because of the reduced number of switchings. The fundamental current however increases gradually from the low frequency to 50 Hz as V/f is maintained constant. After 50 Hz, there is a slight decrease in it, because of the effect of reactance with increase in frequency.

Table 4.1 Modified Switching

V_1	α_1	α_2	α_3
1.10	8.4°	79.15°	82.45°
1.125	8.5°	87.3	90°
1.15	2.7	87.3	90°
1.175	15.7	90.0	90
1.15	18.0	90.0	90
1.20	13.0	90.0	90
1.225	10.0	90.0	90.0
1.25	7.0	90.0	90.0
1.261	5.5	90.0	90.0
1.265	3.0	90.0	90.0
1.273	0.0	90.0	90.0


.9
.7
.5
.3
.1
R = 48
MI = 0.9
or 70.7%
1
48
(e)
.9
.7
.5
.3
.1
R = 96
MI = 0.9
or 70.7%
1
96
(f)

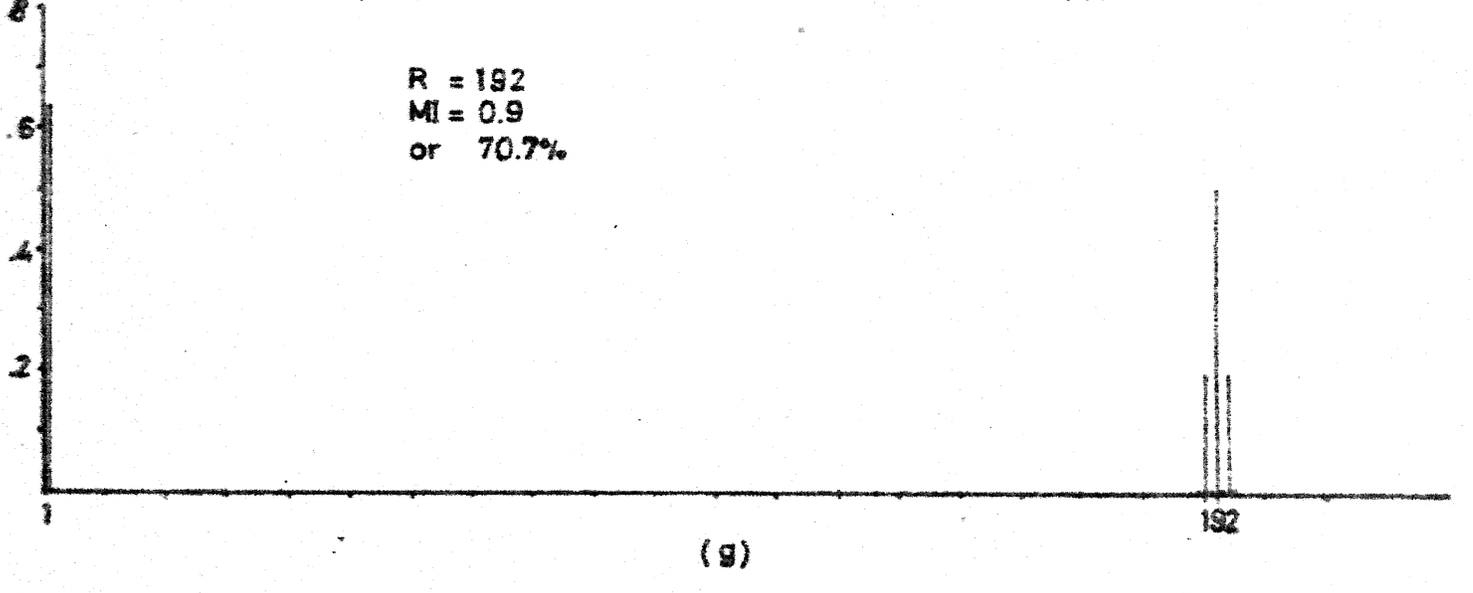

.8
.6
.4
.2
R = 192
MI = 0.9
or 70.7%
1
192
(g)

FIG 4.2 CONTD.

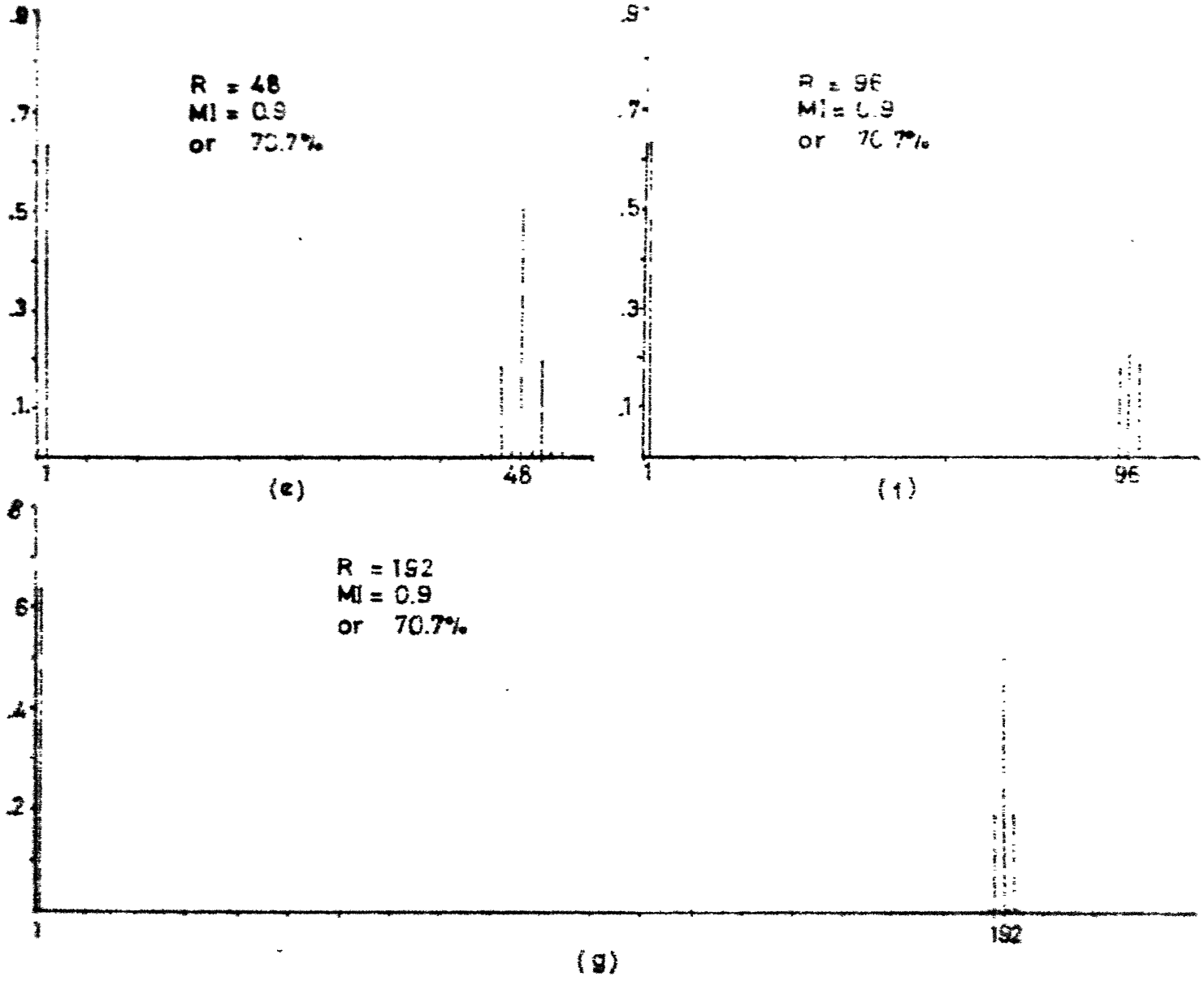

R = 48
MI = 0.9
or 70.7%
1
48
(e)
R = 96
MI = 0.9
or 70.7%
1
96
(f)
R = 192
MI = 0.9
or 70.7%
1
192
(g)

FIG 4.2 CONTD.

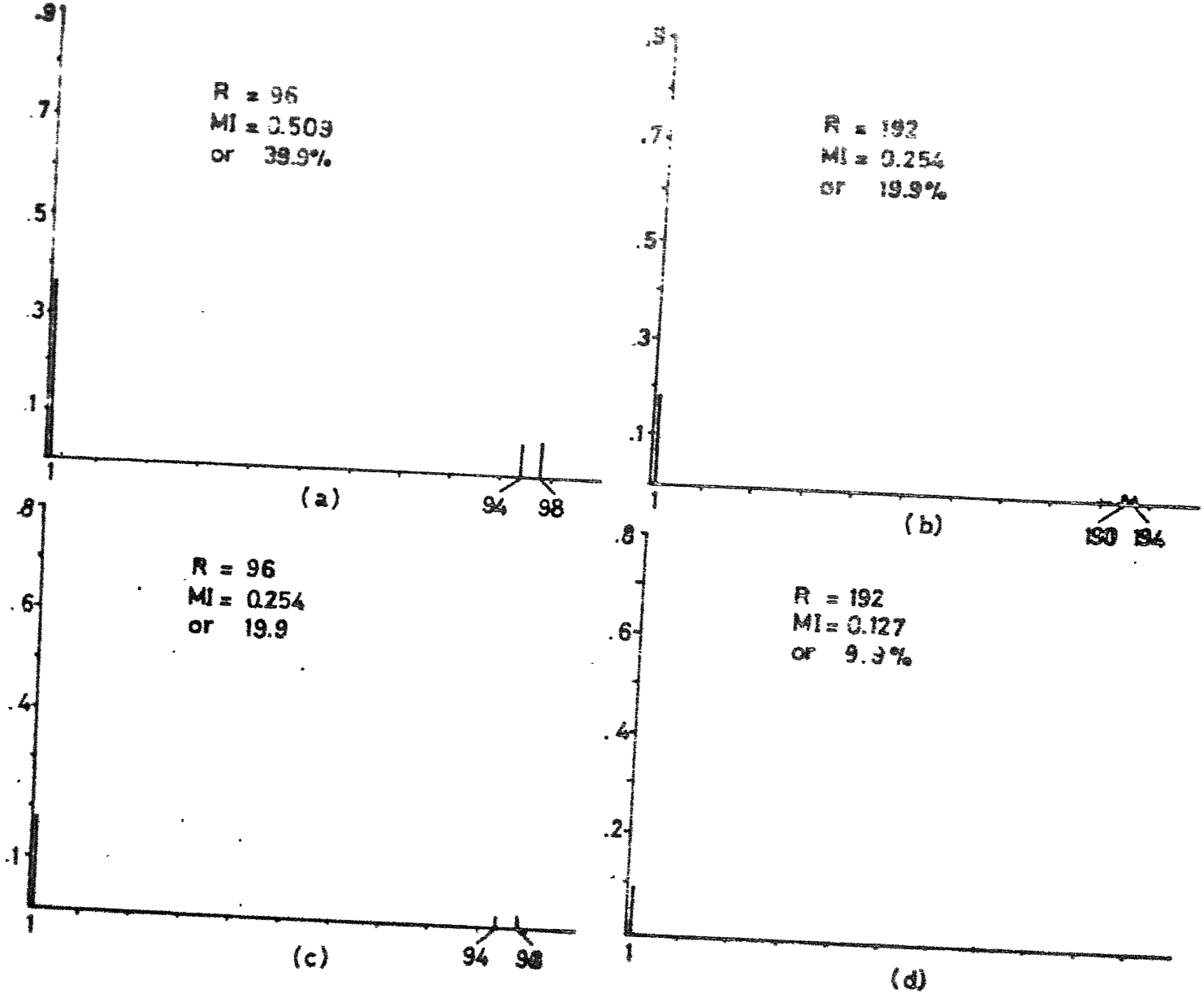


FIG 4.3 3PH SPWM HARMONIC SPECTRUM
(V_ll/2 ph voltage) w/o harm

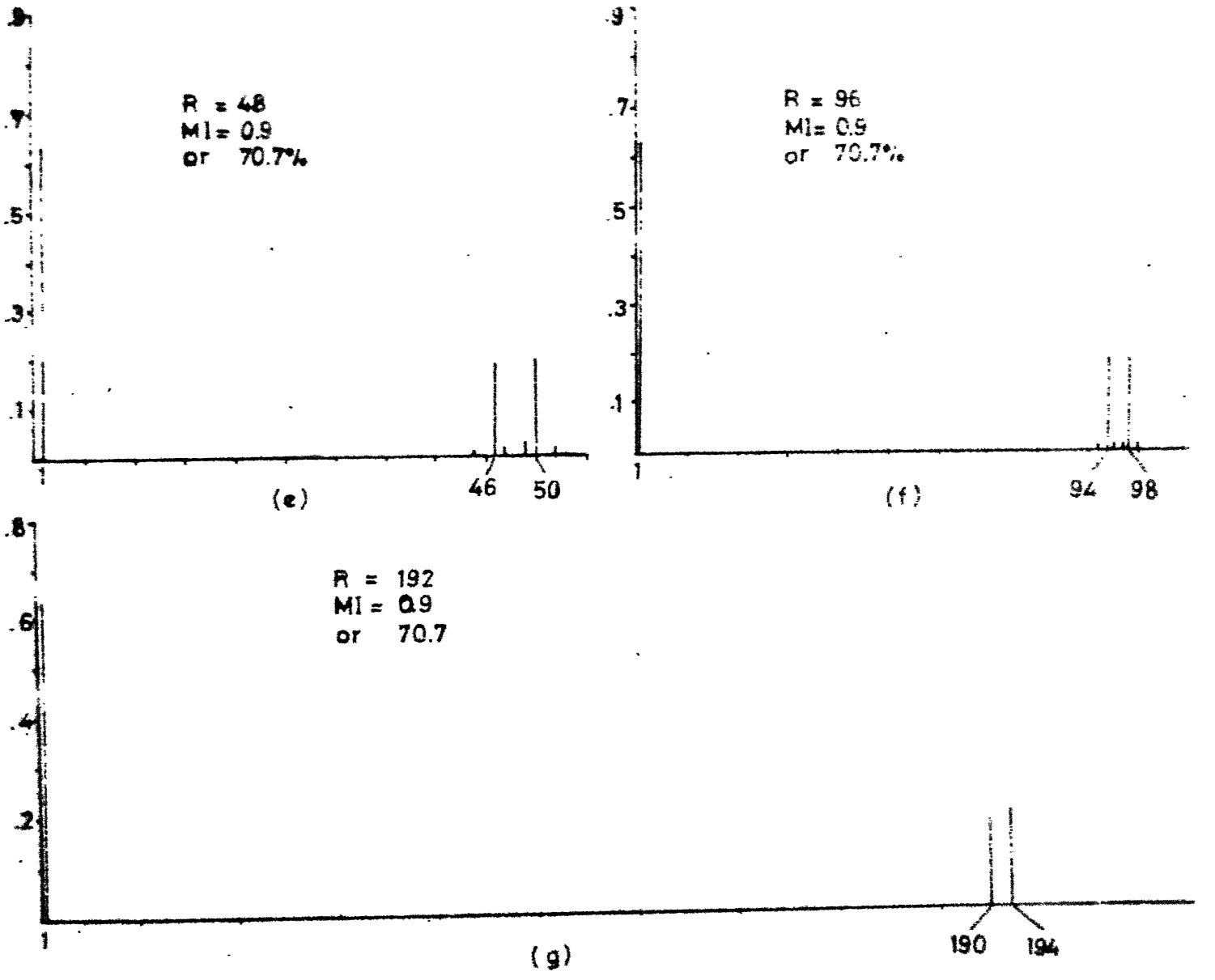

R = 48
MI = 0.9
or 70.7%
46
50
(e)
R = 96
MI = 0.9
or 70.7%
94
98
(f)
R = 192
MI = 0.9
or 70.7
190
194
(g)

FIG 4.3 CONTD

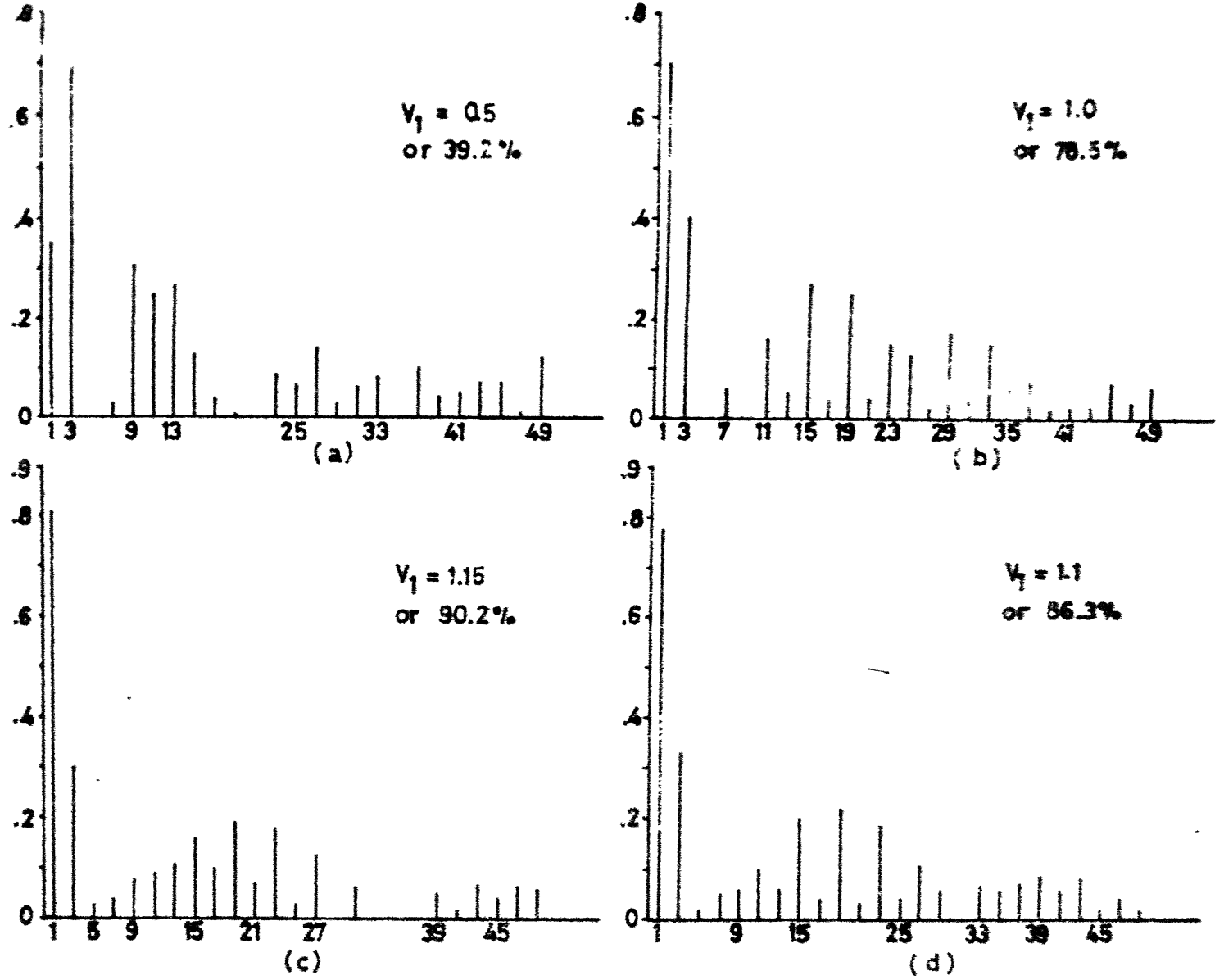


FIG 4.5 OPTIMAL PWM (1PH) HARMONIC SPECTRUM
($V_1\sqrt{2}$ v/s harmonics)

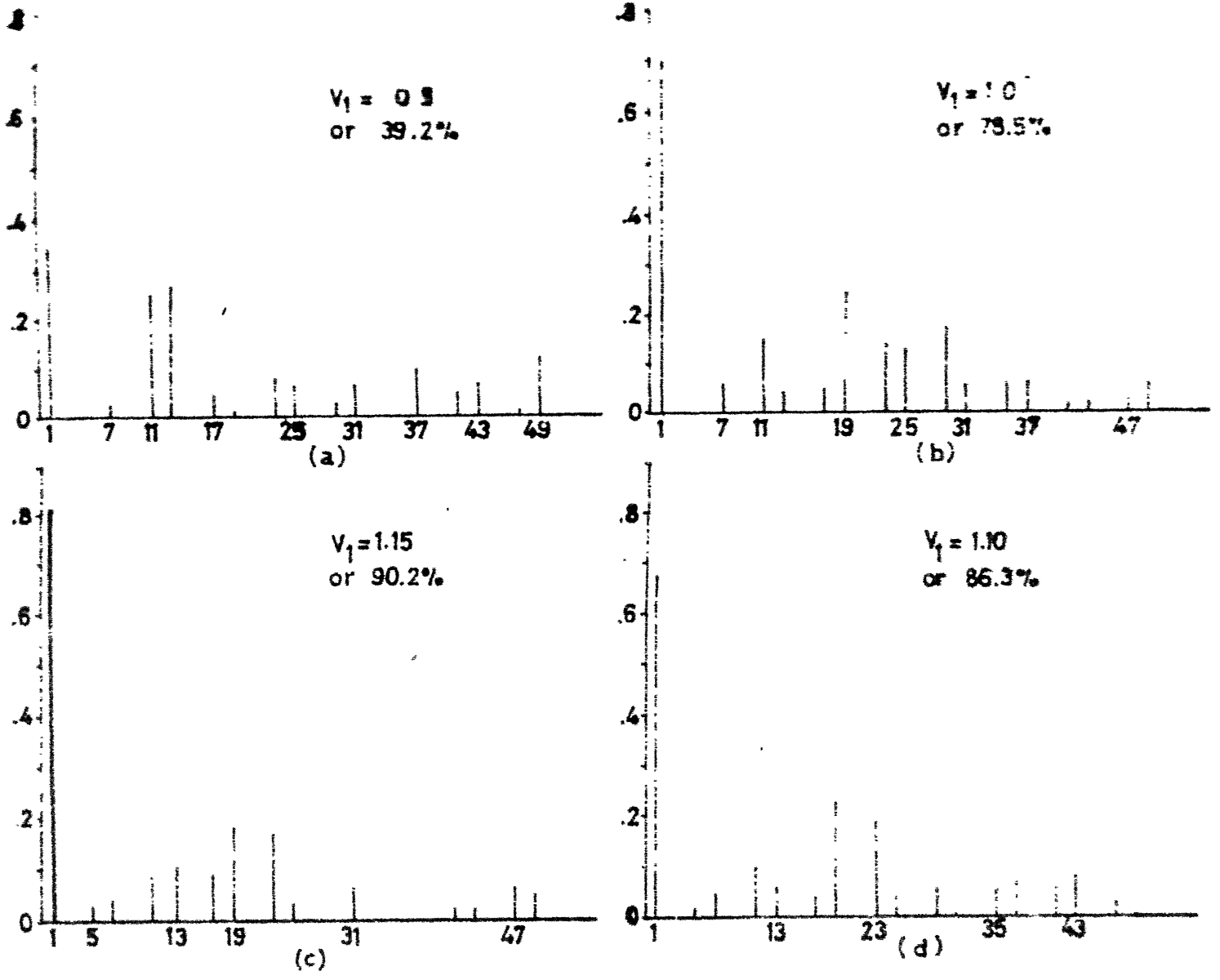


FIG 4.6 3PH OPTIMAL PWM HARMONIC SPECTRUM
(V_1//2(PH. Voltage v/s harmonics)

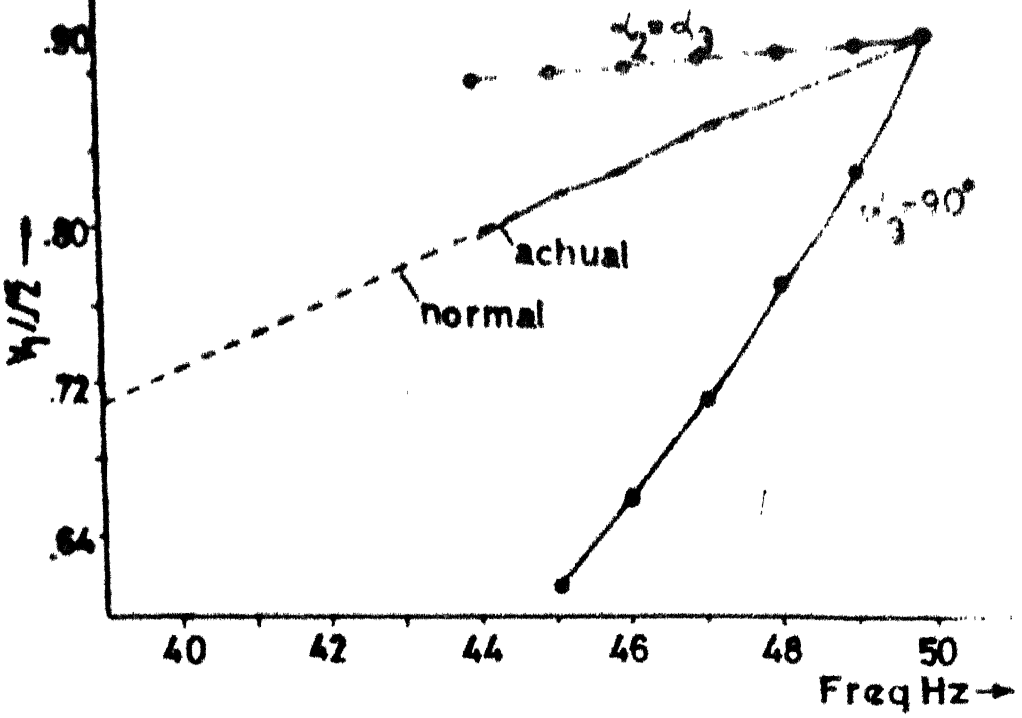

.90
.80
.72
.64
achual
normal
40
42
44
46
48
50
Freq Hz

Fig 4.7

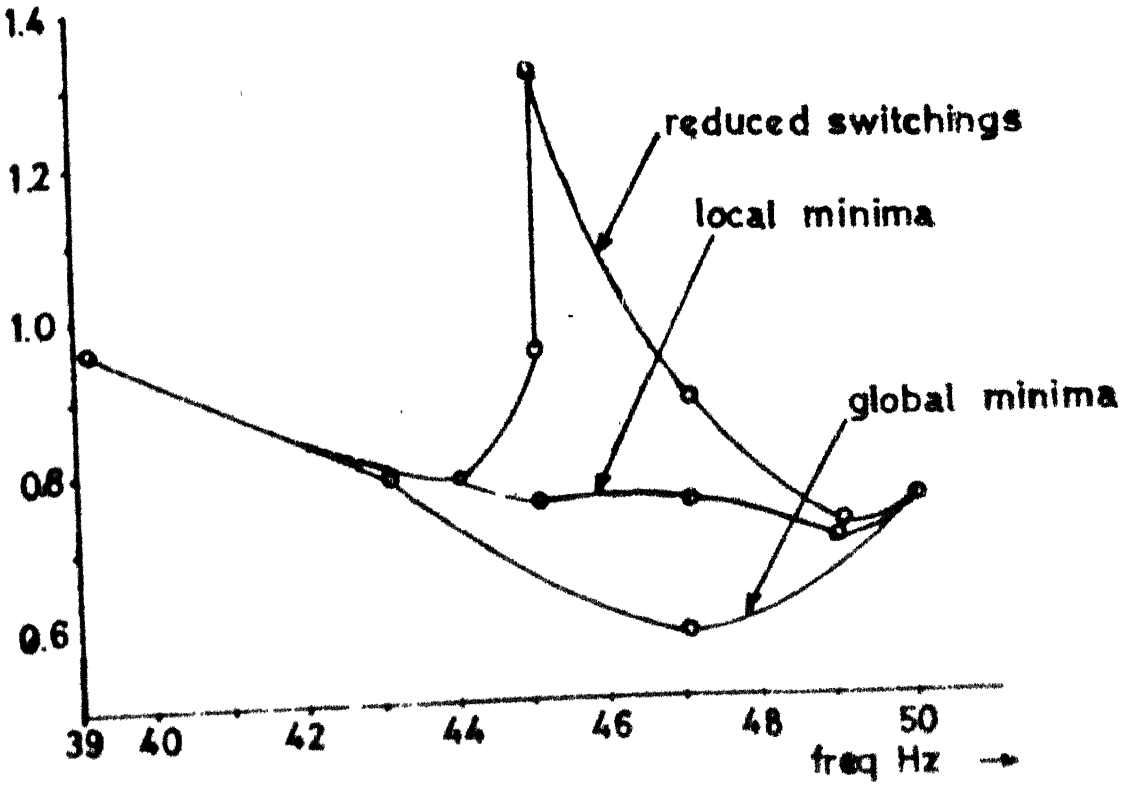

1.4
1.2
1.0
0.8
0.6
reduced switchings
local minima
global minima
39
40
42
44
46
48
50
freq Hz

Fig 4.8

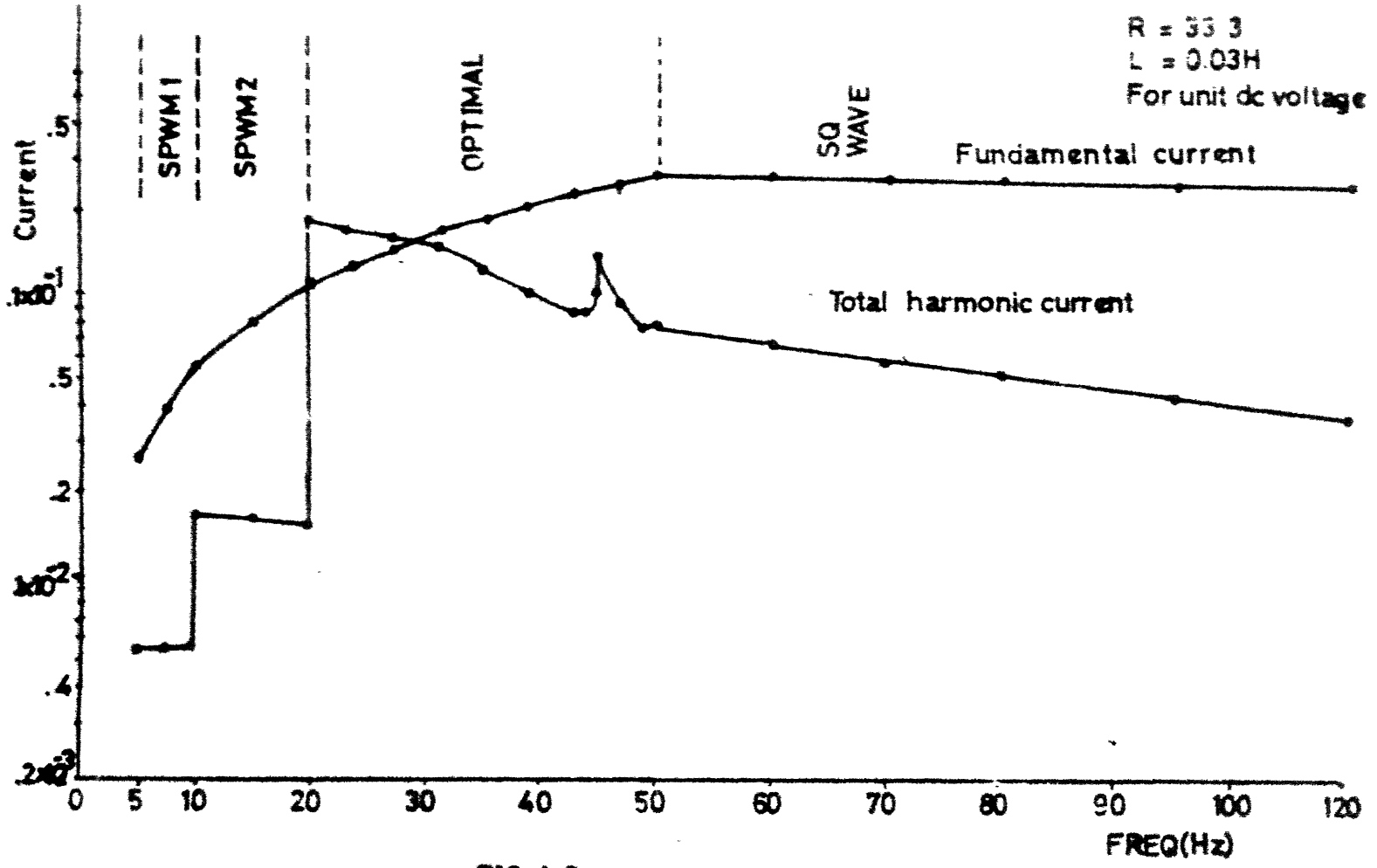

R = 33 3
L = 0.03H
For unit dc voltage
SPWM 1
SPWM 2
OPTIMAL
SQ WAVE
Fundamental current
Total harmonic current
Current
.5
.2
.4
0
5
10
20
30
40
50
60
70
80
90
100
120
FREQ(Hz)

FIG 4.9

CHAPTER 5

TRANSISTOR INVERTER AND EXPERIMENTAL RESULTS

5.1 SELECTION OF DEVICE AND DESIGN OF INVERTER

A power darlington MJ10009 was chosen for designing the inverter. It's internal details are shown in fig. 5.1. It has maximum current and voltage rating of 20A and 500 volts respectively. Because of darlington construction, it has low base drive requirements. The speed up diode helps faster turn off. A fast recovery rectifier between collector and emitter eliminates the necessicity of using external diode, in inverter applications.

5.1.2 Snubber Circuit Design

A safe operating area (SOA) is specified for a power transistor. The operating point of the transistor should lie within this area. If the transistor is reverse biased for faster turn off, then reverse bias safe operating area should be taken into account while designing the snubber circuit (fig 5.3).

A stray inductance (L_s) is invariably present in the circuits. This inductance produces an over shoot in the collector voltage, when the transistor turns off, as shown by dotted lines in fig. 5.4. As a result the operating point goes

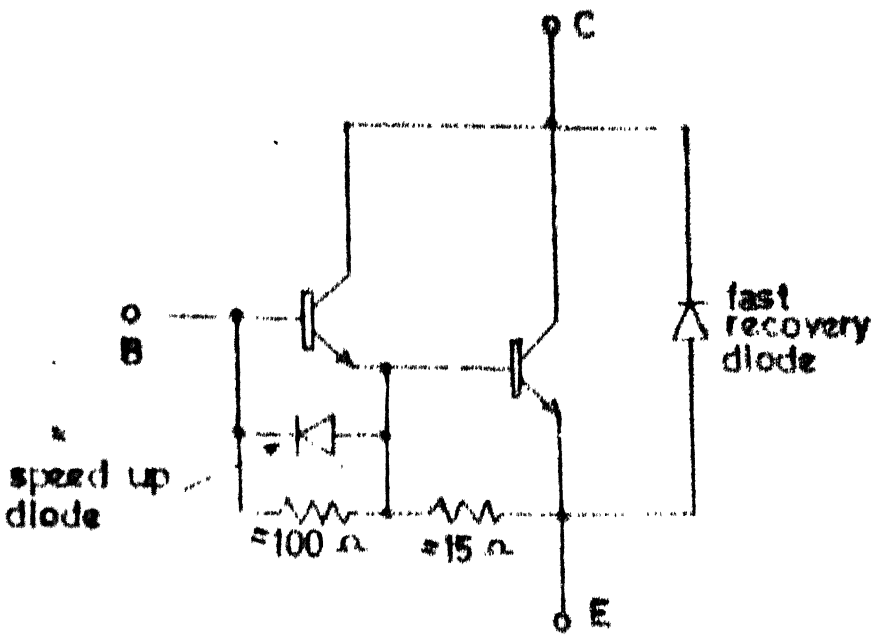


Fig 5 1 MJ 10009

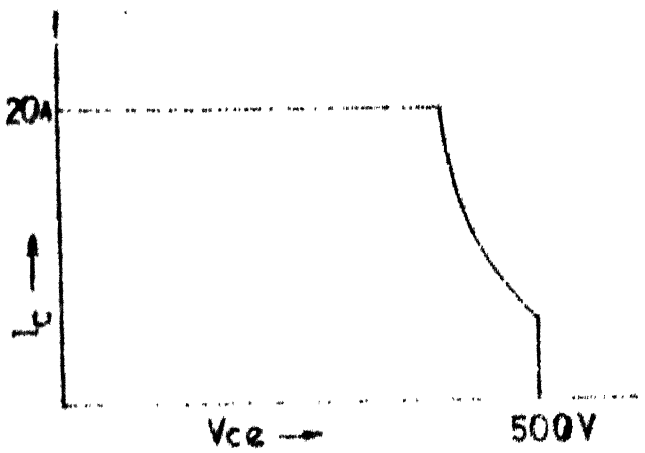


Fig 5 2 RBSOA

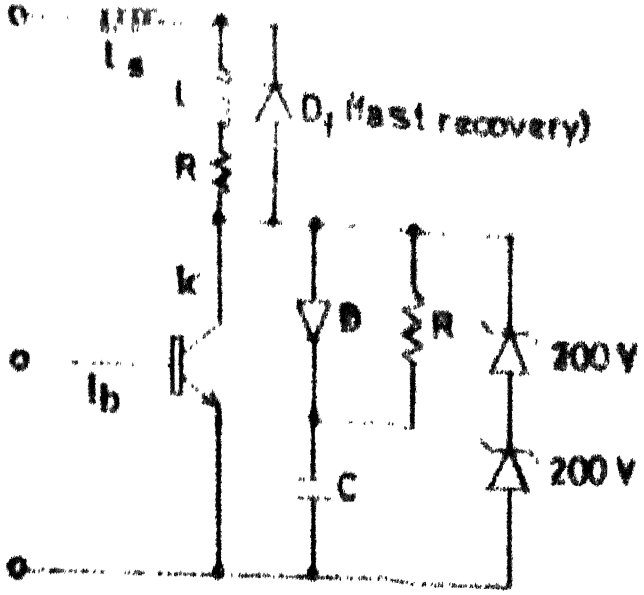


Fig 5.3 TRANSISTOR WITH SNUBBER

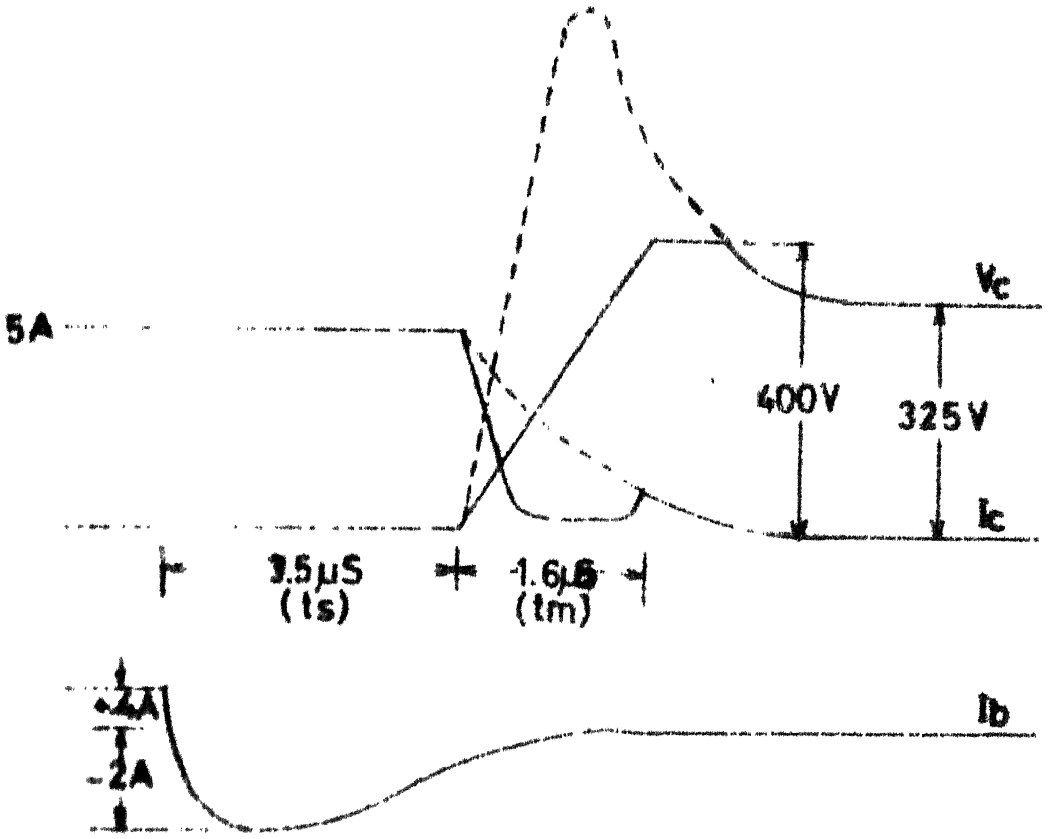


Fig 5.4 TURN OFF PROCESS

out of RBSOA. A snubber circuit if used will restrict the operating point within the RBSOA. Fig 5.3 shows a snubber circuit, and the resulting voltage and current waveforms are as in fig 5.4. The zener clamps the collector voltage within a safe value. The RC snubber with diode D, diverts the collector current from the transistor. In this process the capacitor gets charged, which gets discharged, when the transistor is turned on.

The value of snubber capacitor is given by [17].

$$C = \frac{I_c t_m}{V_2}$$

For V_2 = 400 volts, I_c = 20 Amps and t_m = 1.6 μ sec. The value of C turns out to be 0.08 μF. A capacitor of 0.1 μF was actually used.

The value of R depends upon the minimum on time of the transistor, within which the capacitor has to discharge completely. For a on time of 10 μ sec, the value of R turns out to be 100 Ω.

The power loss in the resistor is given by

$$P = 0.5 \times C \times V_2^2 \, f_{max}$$

With f_{max} of 2000 Hz, the power loss in the resistor is 16 watts.

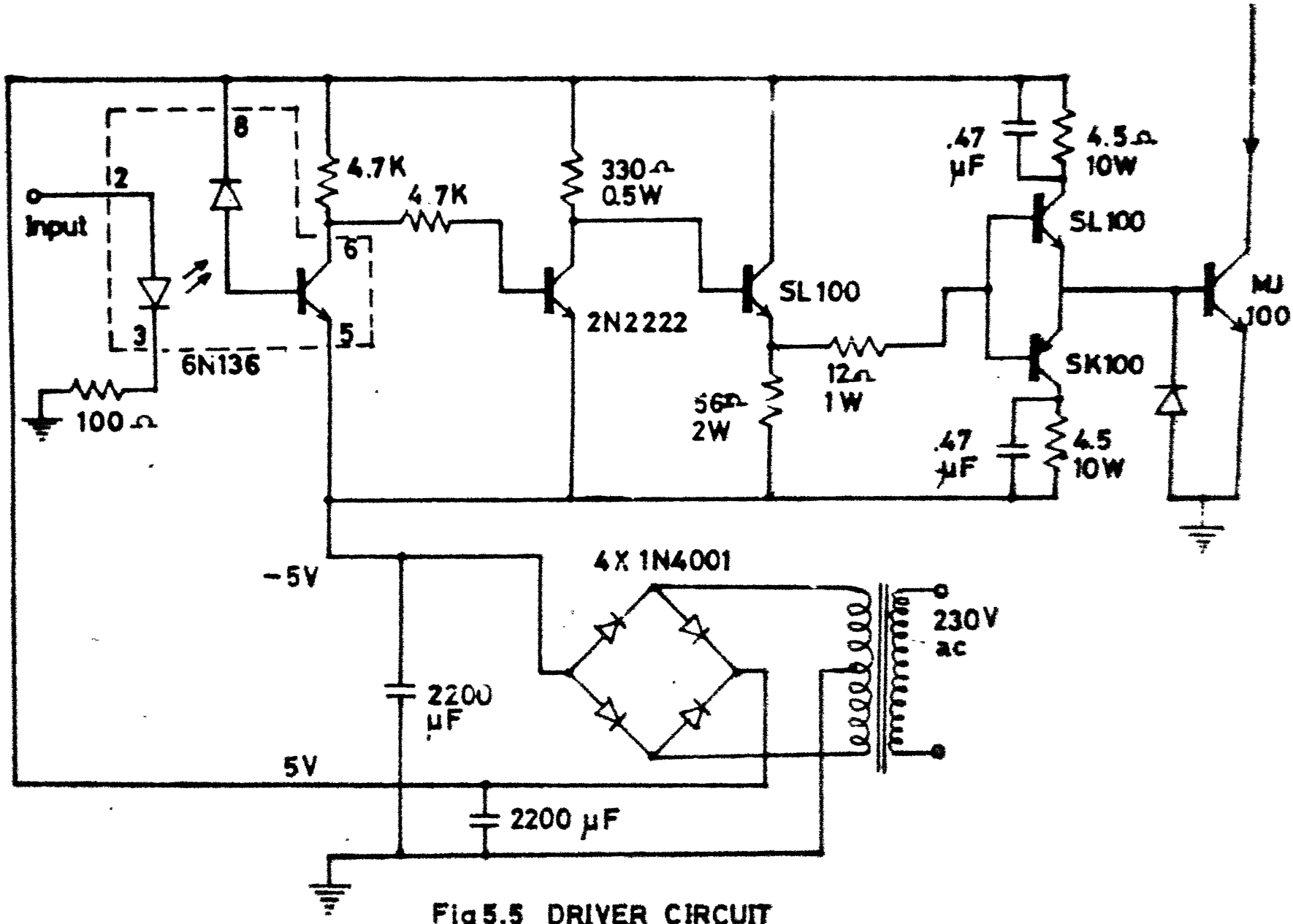


Fig 5.5 DRIVER CIRCUIT

5.1.3 Turn On

In comparison to the turn off, a transistor has a faster turn on. When a transistor turns on, the reverse recovery current of free wheeling diode produces an overshoot in collector current. A fast recovery diode is usually recommended here.

5.1.4 Base Drive

MJ10009, being a darlington transistor, has reasonably high h_{FE}. The drives circuit was designed for a collector current of 10 Amps. At this current, the minimum h_{FE} is 40. The driver stage was designed to give 450 mA drive, using SL100 fig 5.5. It gives an overdrive factor of 2. With the overdriving of base, the operation of transistor in transient condition is reliable and also it reduces steady state losses, due to reduction in $V_{CE(Sat)}$. The capacitors across collector resistors of drive transistor improves the switching.

When the transistor has to be turned off, the base is reverse biased, using SK100. This helps in reducing turn off time of the transistor, by removing the stored charge. The base current waveform during turn off is shown in fig 5.4.

5.1.5 Single Phase Inverter

A single phase inverter was built and tested using the snubber and driver circuits discussed earlier. The circuit

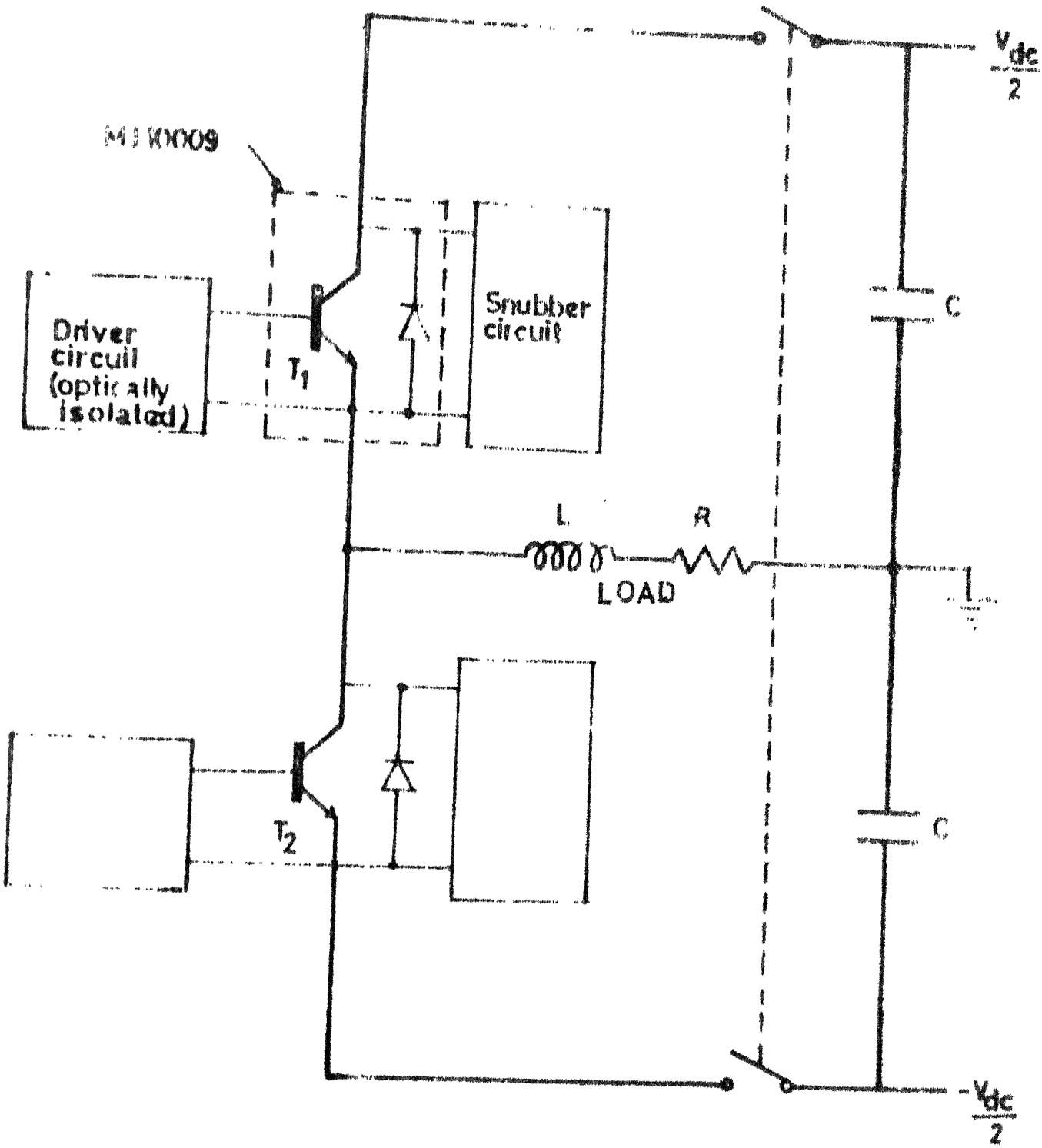


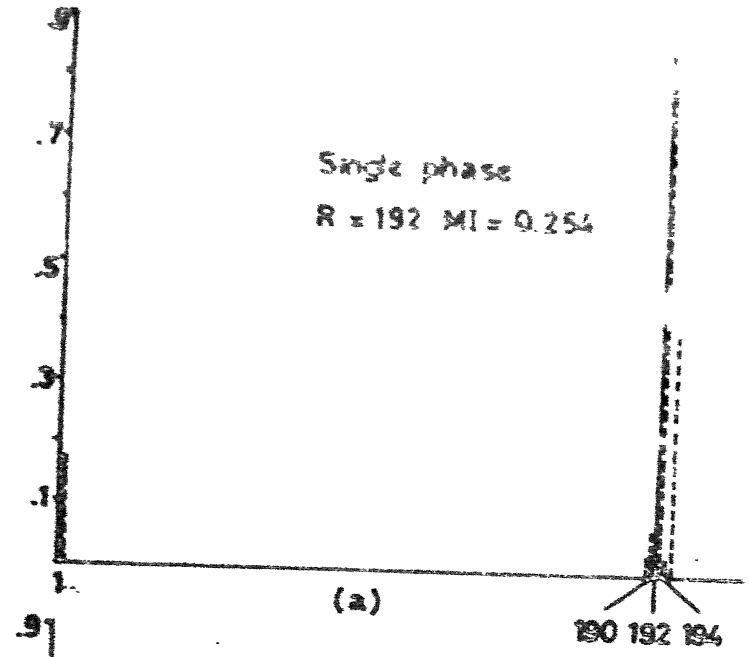
Fig 5.6 TRANSISTOR INVERTER

diagram of this inverter is shown in fig 5.6. When any one of the transistor is turned off a delay has to be provided before the other is turned on, to allow the first one turn off properly. A delay of 10 μ sec was provided in this case.

5.2 RESULTS AND DISCUSSION

The waveforms generated using the modulator were analyzed using a signal analyzer. A comparison of experimental and simulated results of harmonic spectra are given in fig 5.7 and 5.8. Both single phase and three phase waveforms were analyzed. The experimental results are in good agreement with the predicted ones. The slight differences in the amplitudes of the harmonics can be attributed to quantization errors, round off errors. Also the waveforms analyzed had been incorporated with a delay of 10 μ sec as explained in section 3.2.4. Fig 5.9 shows some oscillograms of the experimental results.

A single phase induction motor was run, using the inverter designed in earlier section. The speed torque characteristic is given in fig 5.10. It needs some explaination. The motor could not be loaded properly. Therefore only the input power at the dc link was measured and the torque was calculated (over all system efficiency 0.76). The dc link current has a higher value in optimal region due to large number of harmonics present. Therefore the calculated torque



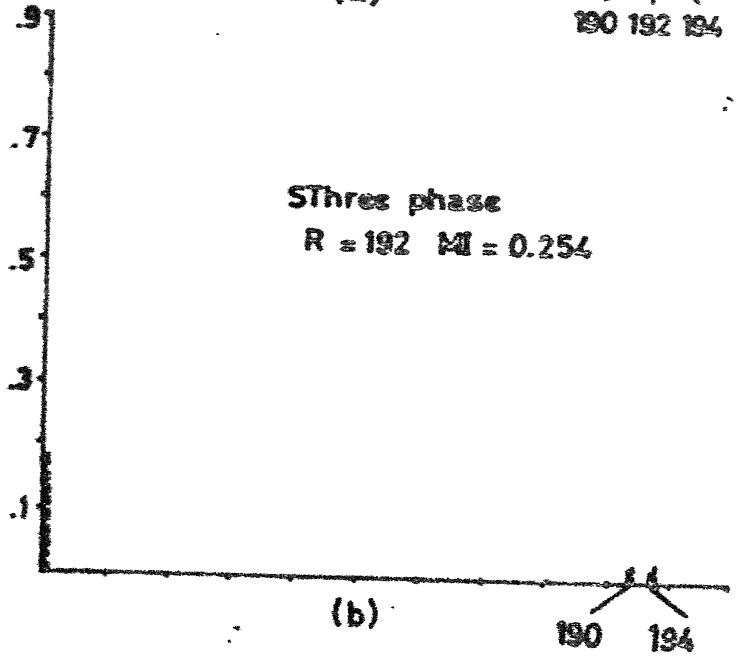
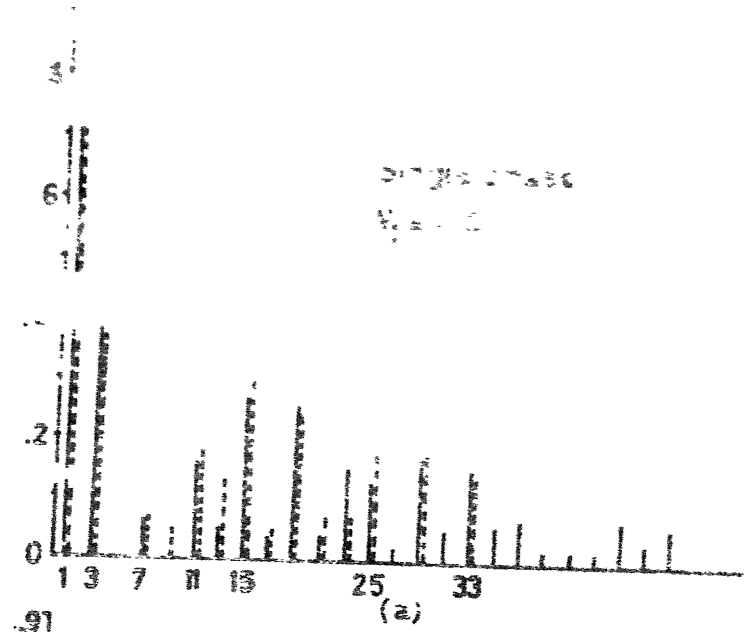


FIG 5.7 SYNC SPWM



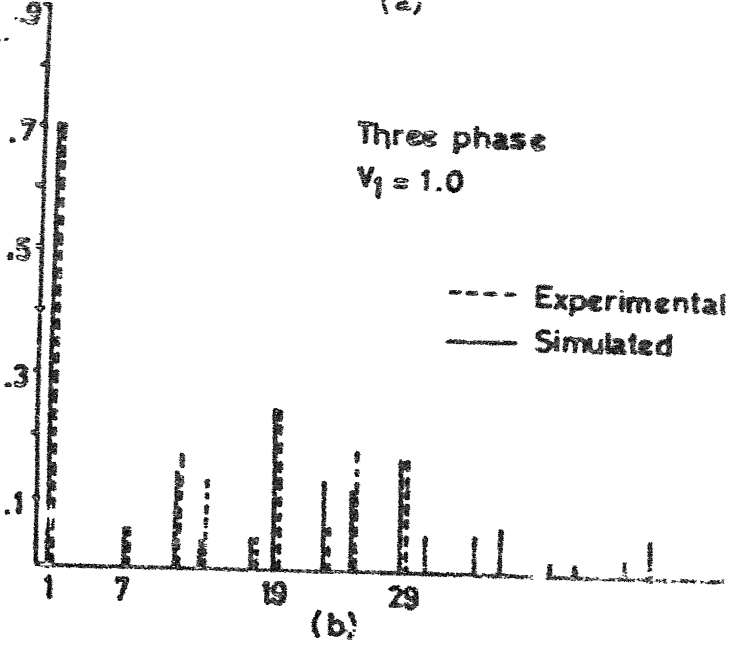
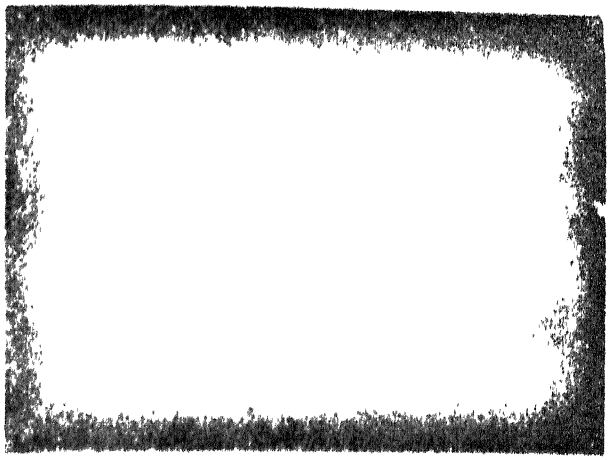
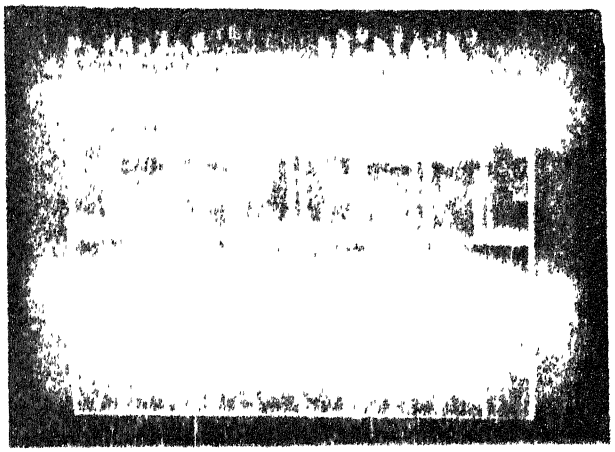


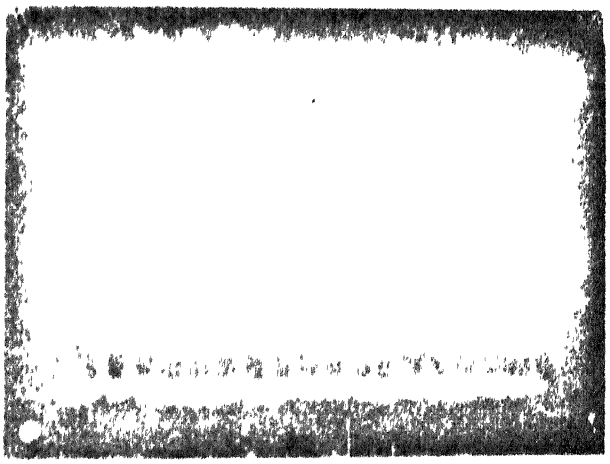
FIG 5.8 OPTIMAL



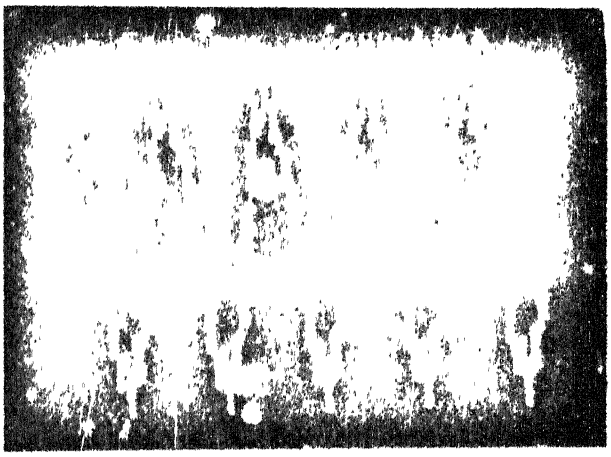
(a) Spectrum for single phase sync SPWM (R = 96, MI = 0.509 or 39.9%)



(b) Single phase optimal PWM (TTL output, V_1 = 1.125 or 86.3%)



(c) Spectrum for single phase optimal PWM (V_1 = 1.0 or 78.5%)



(d) Single phase optimal PWM after filtering the harmonics above 11th (V_1 = 1.0)

FIG 5.9

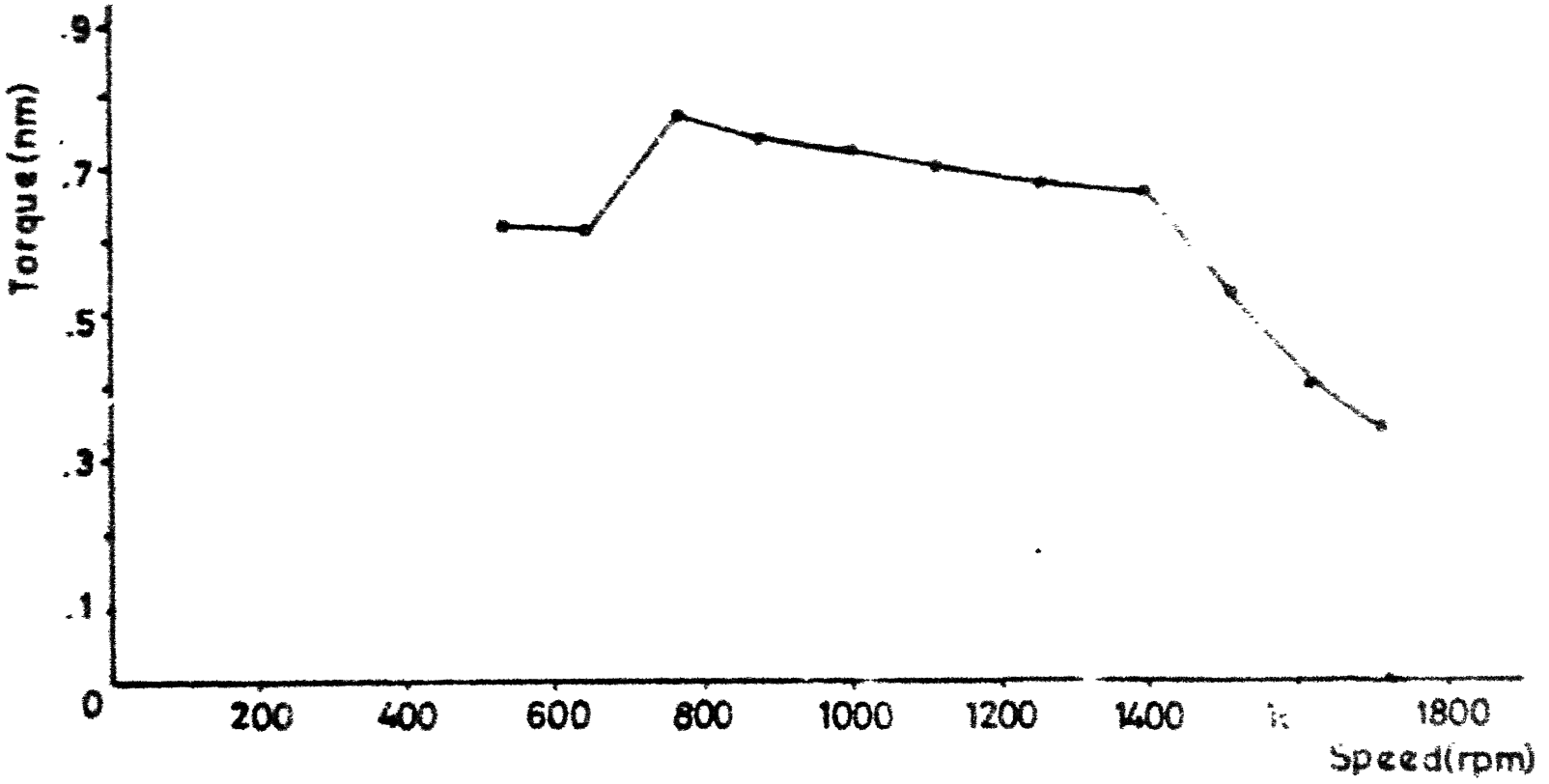


FIG 5.10 SPEED TORQUE CHARACTERSTICS

had this error, and therefore the abnormality in the speed torque characteristic. Due to lack of time no further experimentation could be done.

5.3 CONCLUSION

From chapter 3, it can be concluded that with slight increase in the hardware, it is possible to implement a complex multimode strategy on a slower CPU like 8085. Also some definite CPU time is available for the close loop function.

REFERENCES

1. 'New Sinusoidal pulse width- modulated inverter', Proc IEE 1975, 122 (11) pp 1279-1285.

2. Generalised Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters Part I and II - H.S. Patel and R.G. Hoft IEEE Tran IA Vol IA-9 p 310-317, May/June 1973.

3. Controlled Slip Static Inverter Drive - B. Nokrytzki, IEEE Tran. IGA, Appl. Vol IGA-4, pp 312-317, May/June 1968.

4. Control Strategies for PWM Drives - T.L. Grant and T.H. Barton, Trans IA-16, No. 2, Mar/April 1980.

5. Optimal pulse width modulation for feeding AC motor - G.S. Buja and G.B. Indri,IEEE Trans IA-13, No. 1, Jan/Feb 1977.

6. A High-Performance Pulse-width Modulator for An Inverter Fed Drive System using a Microcomputer - B.K. Bose and H.A. Sutherland, p. 847,IAS 82 Conference record.

7. Microprocessor Control of PWM Inverters - S.R. Bowes, M.J. Mount, IEE Proc. Vol 128 Part B, No. 6,November 1981.

8. An Approach for the Implementation on a Microcomputer of the Control Circuit of Variable Frequency Three Phase Inverters - A. Bellini, C Del, Mastro, G. Figalli, G.Ulivi p 650, IAS 81, Conference record.

9. Microprocessor control system with I/O processing unit LSI for MOTOR drive PWM inverter - S.Moringa, Y.Sugiura et al, p 1197, IAS 81, Conference record.

10. General Purpose Microprocessor Modulator for a wide range of PWM Techniques for AC motor control - F.C. Zach, R.J. Bertnold, K.H. Kaiser, p 446, IAS 82, Conference record.

11. Microprocessor Based Sinusoidal PWM Inverter by DMA Transfer - K.S. Rajashekhara and Joseph Vithayathil - IEEE Transactions on IE, Vol IE 29, No.1 February 1982.

12. Microcomputer Control of PWM Inverters - G.S. Buja, P. Fiorini - IEEE Transactions on IE, Vol IE-29, No.3,Aug 1982.

13. A microcomputer based control signal generator for A three phase switching power inverter - M. Varnovitsky, p 836, IAS 82, Conference record.

14. Computer aided design of PWM inverter systems - S.R.Bowes, R. Clement, IEE proc. Vol 129, pt B, Jan 1982.

15. Digital computer simulation of variable speed PWM inverter machine drive, ibid Vol 130, pt B, No.3, May 1983.

16. Control loop study of induction motor drives using DQ model - Mac Donald - P.C. Sen, IAS 78.

17. Power transistors for chopper and inverters - An application review - B.R. Pelly and J.P. Shen, International Rectifier Elsegundo California.

18. Application of high voltage darlington transistors in ac motor controls - Ralph E Locher, IAS 62: 30A, p 736.

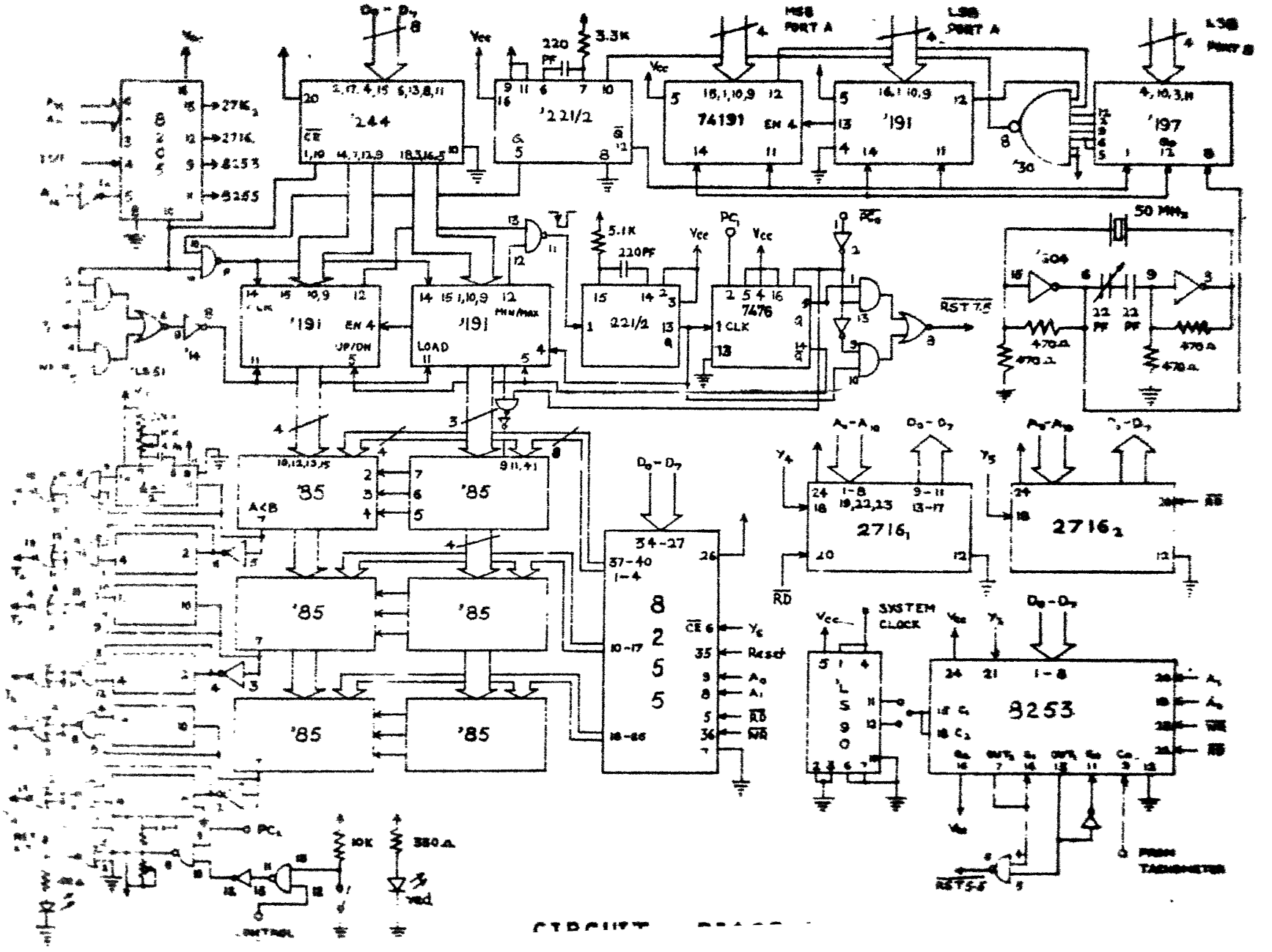
19. Transistorised PWM inverter induction motor drive system - S.C. Peak and A.B. Plunkett, IAS 82:33F, p 892.

20. Printed Circuit Boards Design and Technology - Bosshart, CEDT Series TMH 1983 (Book).

APPENDIX A

CIRCUIT DIAGRAM

All the hardware required except the CPU and RAM was put an one PCB. The CPU and the RAM was used from the intelligent terminal developed in the department. The PCB made directly fits into the edge connector for the processor bus. The layout of the PCB was done using three layer method and according to CEDT standards [20].


'244
'221/2
74191
'191
'30
'197
'191
'191
'221/2
7476
'85
'85
'85
'85
8255
2716₁
2716₂
8253
'LS90
'LS51
'14
'304
50 MHz
5.1K
220PF
3.3K
220 PF
10K
330 Ω
RST 7.5
SYSTEM CLOCK
RD
WR
CONTROL
FROM TACHOMETER

APPENDIX C

OPTIMAL SWITCHING INSTANTS

Modulation : 3 phase for half-bridge (two levels)

Switching numbers in $\pi/2$: 3,

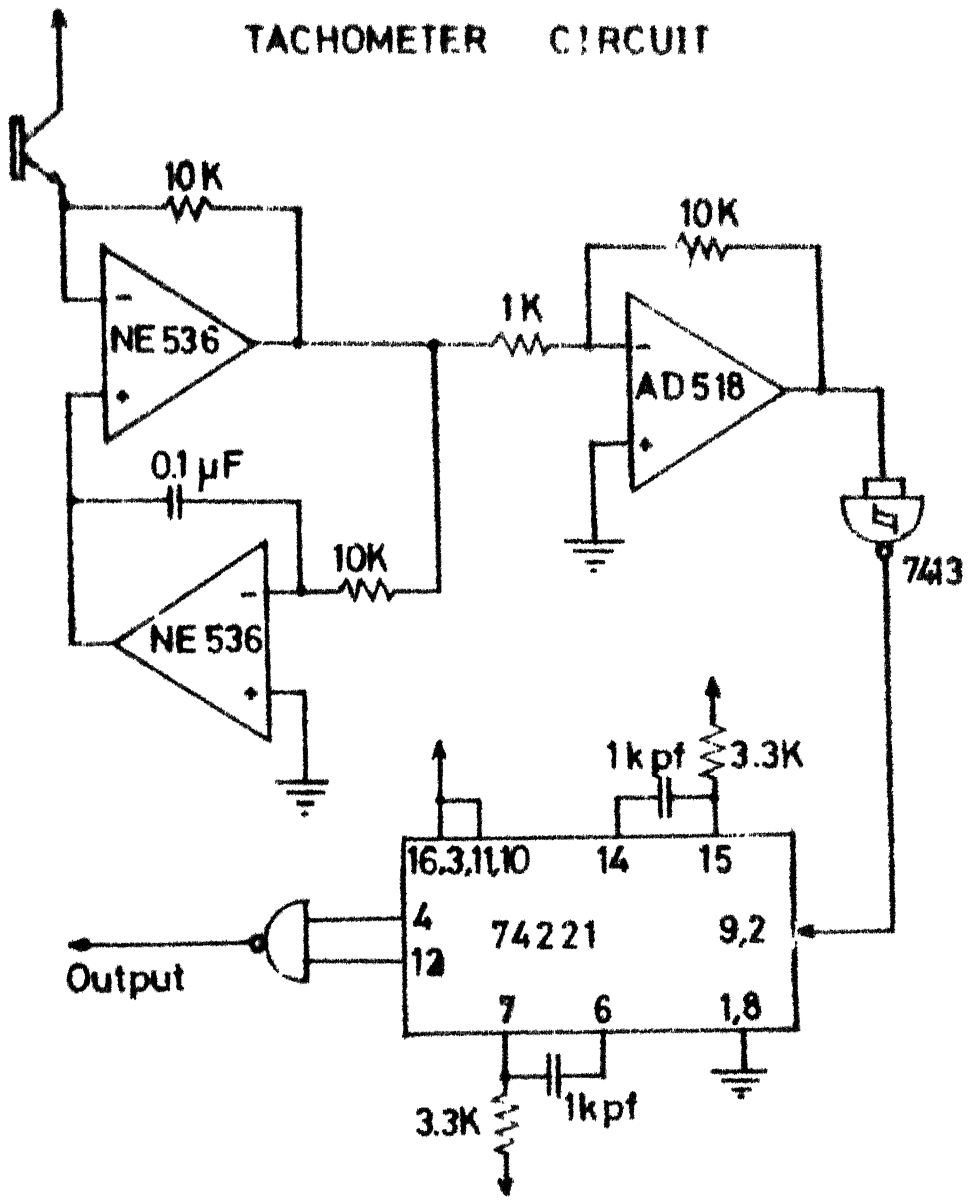
First interval voltage : negative

V_1	α_1	α_2	α_3
0.0	0.00	60.00	90.0
0.1	0.62	61.31	88.89
0.2	1.29	62.63	87.79
0.3	1.60	63.00	85.86
0.4	2.75	65.38	85.71
0.5	3.53	66.82	84.73
0.6	4.34	68.32	83.81
0.7	5.17	69.91	82.97
0.8	6.01	71.65	82.27
0.9	6.86	73.60	81.78
1.0	7.66	75.92	81.67
1.05	8.03	77.34	81.88
1.10	8.37	79.05	82.38
1.15	8.64	81.29	83.43
1.20	6.45	17.06	21.00
1.25	3.39	7.75	10.43
1.27	1.19	2.52	3.65

APPENDIX D

CONSTRUCTION OF OPTICAL TACHOMETER

A disc with 720 lines was mounted on the motor shaft. The signal from the interrupter module was processed using FET input op amp. Both the rising and falling edge of the output was used to generate one pulse each. Thus getting 1440 pulses per rpm. The circuit diagram of the processing stage is given here.


TACHOMETER CIRCUIT
10K
NE 536
1K
10K
AD 518
0.1 µF
10K
NE 536
7413
1kpf
3.3K
16,3,11,10
14
15
4
12
74221
9,2
Output
7
6
1,8
3.3K
1kpf